Abstract: A new compact model for MOS transistors has been developed, MOS Model 11 (MM11), the successor of MOS Model 9. On April 16th, 2002, a MOS Model 11 workshop was organized by MOS4YOU (J. Knol) in co-operation with the NatLab. Three lectures were given, dealing with:

- the physical background of MM11
- the parameter extraction for MM11
- RF-CMOS models based on MM11

The slides used for the last topic are classified, and can be found in NL-TN2002/168. This report consists of the copies of the slides used in the first two presentations.
Introduction: MOS Model 11

Goals for MOS Model 11 (MM11):

- suitable for digital, analog and RF
- suitable for modern/future CMOS processes
- physics based
- simulation time comparable to MM9
- number of parameters comparable to MM9
- simple parameter extraction
Model developed for accurate distortion analysis in circuit design:

- surface-potential-based model
  - accurate transition weak → strong inversion
- symmetrical
- distortion
  - accurate description of third-order derivatives (i.e. $\frac{\partial^3}{\partial V^3}$)

implemented physical effects:

- mobility reduction
- bias-dependent series-resistance
- velocity saturation
- conductance effects (CLM, DIBL, etc.)
- gate leakage current
- gate depletion
- quantum-mechanical effects
- bias-dependent overlap capacitances
MOS Model 11: Physical Background

Introduction: structure of MOS Model 11

- Junction diodes modelled by JUNCAP-model
- Geometry Scaling
- Temperature Scaling
- Model Equations
- Currents Charges Noise

Physical background: outline

- Introduction
- DC-Model
- AC-Model
- Noise Model
- Summary
DC-Model: MOS physics

**accumulation**  $V_{GS} < V_{FB} \approx -1 \text{ V}$  
**depletion or weak inversion**  $V_{FB} < V_{GS} < V_{T}$  
**strong inversion**  $V_{GS} > V_{T}$

![Diagrams showing accumulation, depletion, and strong inversion](image1)

DC-Model: $V_T$-based model

intrisic MOS behaviour + overlap regions described by MOS Model

\[ Q_{inv} \approx -C_{ox} \cdot (V_{GS} - V_T) \]
\[ I_{DS} = -\mu \cdot W \cdot Q_{inv} \cdot \frac{\partial V}{\partial x} \]
DC-Model: \( V_T \)-based model

\[ I_{DS} \propto \exp\left(\frac{V_{GS} - V_T}{m \cdot \varphi_T}\right) \]

\( V_T \)-based model:

interpolation needed between subthreshold and superthreshold
(e.g. BSIM4 and MM9)

Smoothing function

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DC-Model: \( V_T \)-based model (MM9)

Smoothing function in MOS Model 9
(NMOS, \( V_{DS}=50 \text{ mV} \), \( V_{SB}=0 \text{ V} \), \( W/L=10/10 \mu\text{m} \))

\[ I_D (\mu\text{A}) \]

\[ V_{GS} (\text{V}) \]

\( \zeta=0.3 \quad \zeta=1.0 \quad \zeta=3.0 \)

\[ g_m (\mu\text{A/V}) \]

\[ V_{GS} (\text{V}) \]

Drain current

Transconductance

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Let's make things better
**MOS Model 11: Physical Background**

**ψ_s-based model:**

Single equation for whole operation range:

\[
I_{\text{drift}} = f(V_{GB}, \psi_s, \psi_L) \]

\[
I_{\text{diff}} = g(V_{GB}, \psi_s, \psi_L) \]

\[
I_D = I_{\text{drift}} + I_{\text{diff}} \]

---

**DC Model: surface potential ψ_s**

Electrostatic potential at oxide interface w.r.t. bulk:

\[ V_{GB} > V_{FB} \]

\[ \psi_s = 2\psi_F \]

\[ N_d = 2 \times 10^{17} \text{ cm}^{-3} \]

\[ t_{ox} = 3.2 \text{ nm} \]

---

Let's make things better.
**DC Model: surface potential $\psi_s$**

### Quasi-Fermi Potential $V$

- $V = V_{SB}$ at Source
- $V = V_{DB}$ at Drain

**Graph:**
- $t_{ox} = 3.2 \text{ nm}$
- $N_A = 2 \times 10^{17} \text{ cm}^{-3}$
- $V = 1 \text{ V}$
- $V = 0 \text{ V}$
- $\psi_s = 2\psi_0 + V'$

**Equations:**
- $V_{GB}$
- $q \cdot \psi_s$
- $V$

**Diagram Elements:**
- Gate Oxide
- Substrate
- $E_C$
- $E_F$
- $E_I$
- $E_V$

---

**DC-Model: surface-potential-based model**

- $I_{diff} = -\mu \cdot W \cdot Q_{inv} \cdot \frac{\partial \psi_s}{\partial x}$
- $I_{drift} = \mu \cdot \varphi_T \cdot W \cdot \frac{\partial Q_{inv}}{\partial x}$
- $I_{DS} = I_{drift} + I_{diff}$

**Equations:**
- $Q_{inv} = -C_{ox} \cdot (V_{GB} - V_{FB} - \psi_s - k_0 \cdot \sqrt{\psi_s})$
- $Q_{dep} \approx -C_{ox} \cdot k_0 \cdot \sqrt{\psi_s}$
**MOS Model 11: Physical Background**

DC-Model: drift and diffusion components

$I_D - V_{GS}$ at $V_{DS} = 1$ V

![Graph](image1)

**Surface Potential**

**Drain Current**

DC-Model: linear/saturation region

$I_D - V_{DS}$ at $V_{GB} - V_{FB} = 2$ V

![Graph](image2)

**Surface Potential**

**Drain Current**

Let's make things better

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DC-Model: surface potential approximation

\[
\left( \frac{V_{GB} - V_{FB} - \psi_s}{k_0} \right)^2 = \psi_s + \varphi_T \cdot e^{-\frac{\varphi_T}{\psi_s}} \cdot \left( e^{\frac{\psi_s}{\varphi_T}} - 1 \right) + \varphi_T \cdot \left( e^{\frac{\psi_s}{\varphi_T}} - 1 \right)
\]

\[ \Rightarrow \text{iterative solution} \]
\[ \Rightarrow \text{time consuming} \]
\[ \Rightarrow \text{approximation used:} \]
\[ \psi_s = \psi_s(V_{GB}, V) \]

(Solid-State Electron. 44, 2000)

---

DC-Model: surface potential → threshold voltage

Although in a \( \psi_s \)-based model no threshold voltage \( V_T \) is used, it can be calculated by:

\[
V_T = V_{FB} + \psi_0 + k_0 \cdot \sqrt{\psi_0} + V_{SB}
\]

where: \( \psi_0 = \varphi_B + 2 \cdot \frac{k_B \cdot T}{q} \)

And \( V_{FB}, k_0 \) and \( \varphi_B \) are model parameters.
Description of ideal long-channel MOSFET

For real devices several physical effects have to be taken into account:

- mobility effects
- conductance effects

New models

Special attention to:

- distortion
- drain-source symmetry

DC Model: distortion behavior

- 2nd-order distortion: cancels out in balanced circuit
- 3rd-order distortion: limits dynamic range

⇒ accurate description of 3rd-order derivatives
Outline: DC-Model

- $V_T$ vs. $\psi_s$-based models

**Mobility reduction**
- Bias-dependent series-resistance
- Velocity saturation
- Conductance effects
- Symmetry
- Gate leakage current

DC-Model: mobility reduction

**MOS Model 9:**

$$\mu = \frac{\mu_0}{1 + \theta \cdot E_{eff}}$$

higher-order derivatives:

$$g_{mi} = \frac{\partial^i I_D}{\partial V_{GS}}$$

not well described
DC-Model: mobility reduction

- surface roughness scattering:
  \[ \mu_{sr} \propto E_{eff}^{-2} \]

- phonon scattering:
  \[ \mu_{ph} \propto E_{eff}^{-\frac{2}{3}} \]

\[ \mu = \frac{\mu_0}{1 + \sqrt{\theta_{sr} \cdot E_{eff}^4 + \theta_{ph} \cdot E_{eff}^{2/3}}} \]

(IEEE TED-44, No. 11, p. 2044, 1997)

\[ \Rightarrow \text{different for holes} \]

DC-Model: bias-dependent series-resistance

internal series-resistance:

- bias-dependent for LDD-MOSFETs
- independent parameters:
  \[ \theta_R = 2 \cdot \beta \cdot R_{series} \]

Gate-bias induced distortion for NMOS, W/L=10/1\(\mu\)m

Harmonic Amplitude (A)

Mobility Reduction and Series-Resistance
**MOS Model 11: Physical Background**

**Electron velocity:**

\[ v = \frac{\mu \cdot E_{||}}{\sqrt{1 + \left(\frac{\mu}{v_{sat}} \cdot E_{||}\right)^2}} \]

- **Approximation used in calculation of \( I_{DS} \):**
  - Electric field \( E_{||} \) varies linearly along channel.

**Carrier velocity**

(MM9, BSIM4):

\[ v = \frac{\mu \cdot E_{||}}{1 + \mu \cdot E_{||} / v_{sat}} \]

**Drain current:**

\[ I_{DS} = -W \cdot Q_{inv} \cdot v \]

**Harmonic Amplitude (A)**

- Harmonic Amplitude (A) is depicted against different voltages.
- Different curves represent different bias conditions.

**Electric field \( E_{||} \):**

\[ E_{||} = \frac{2 \cdot (V_{SL} - V_{SG})}{L} \]

**Channel length**

- Channel length \( L \) is illustrated.

**Let's make things better**

**PHILIPS**
Drain-bias induced distortion for NMOS W/L=10/1μm

- Velocity Saturation
- Channel Length Modulation
- V_{DS} (V)
- Static Feedback and Self-Heating
- Weak-Avalanche

Outline: DC-Model

- V_T vs. \psi_S-based models
- Mobility reduction
- Bias-dependent series-resistance
- Velocity saturation
- Conductance effects
- Symmetry
- Gate leakage current
DC-Model: drain-source symmetry

Symmetry w.r.t. source and drain at $V_{DS} = 0$

⇒ MOS models developed for $V_{DS} \geq 0$

⇒ for $V_{DS} < 0$, source & drain are interchanged

In order to preserve symmetry:

$$I_{DS}(V_{GS}, V_{DS}, V_{SB}) = -I_{DS}(V_{GD}, V_{SD}, V_{DB})$$

Care has to be taken with the implementation of:

- ideal current equation
- velocity saturation
- DIBL/static feedback
- smoothing function (linear/saturation region)

Not valid for threshold-voltage-based models
MOS Model 11: Physical Background

\[ I_{DS}(V_{GS}, V_{DS}, V_{SB}) = -I_{DS}(V_{GD}, V_{SD}, V_{DB}) \]

Care has to be taken to preserve symmetry

Outline: DC-Model

- \(V_T\) vs. \(\psi_s\)-based models
- Mobility reduction
- Bias-dependent series-resistance
- Velocity saturation
- Conductance effects
- Symmetry
- Gate leakage current
Simplified relation:

\[ J_G \propto J_0 \cdot \exp(B \cdot V_{GS}) \]

where:

\[ J_0 \propto \frac{1}{t_{ox}^2 \cdot \exp(t_{ox})} \]
MOS Model 11: Physical Background

**NMOS (in inversion):**

Gate current density:

\[ J_G \propto Q_{inv} \cdot P(V_{ox}) \]

Approximation (at \( V_{DS}=0 \) V):

\[ I_G = I_0 \cdot V_{ox} \cdot Q_{inv} \cdot e^{B_0 V_{ox}} \]

**DC-Model: gate leakage model**

**DC-Model: gate current components**

NMOS, \( t_{ox}=2 \) nm, Area=6 \( \mu \)m²
DC-Model: gate current components

\[ V_{gs} > 0 \]

\[ I_G \]

\[ I_{GOV} \]

\[ V_{gs} (V) \]

\[ I_g (A) \]

\[ I_{GS} + I_{GD} \]

Parameter \( I_{GOV} \)

\[ Measurments \]

MM11

\[ V_{gs} (V) \]

\[ I_g (A) \]

\[ I_{GS} + I_{GD} \]

NMOS, \( t_{ox} = 2 \) nm, Area=6 \( \mu m^2 \)

DC-Model: gate current components

\[ V_{gs} < 0 \]

\[ I_G \]

\[ I_{GOV} \]

\[ V_{gs} (V) \]

\[ I_g (A) \]

\[ I_{GS} + I_{GD} \]

Parameter \( I_{GOV} \)

\[ Measurments \]

MM11

\[ V_{gs} (V) \]

\[ I_g (A) \]

\[ I_{GS} + I_{GD} \]

NMOS, \( t_{ox} = 2 \) nm, Area=6 \( \mu m^2 \)
DC-Model: gate current components

NMOS, $t_{ox}=2$ nm, Area=6 $\mu$m$^2$

Let's make things better
**DC-Model: gate leakage model**

\[ I_{GC} = I_o \cdot \int V_{ox} \cdot Q_{nv} \cdot e^{\frac{I_{ox} V_{ox}}{d_L}} \]

- Determined by overlap region.
- Determined by intrinsic region.

**Gate current may affect off-current for future CMOS**

PMOS, \( V_{DS} = 1.5 \text{V}, t_{ox} = 1.9 \text{nm}, W/L = 10/0.13 \mu\text{m} \) (CL013G)
DC-Model: gate current partitioning

\[ I_{GD} = W \cdot \int_{x/L} J_G \cdot dx \]
\[ I_{GS} = I_G - I_{GD} \]

\( I_{GD}/I_{G} \), \( I_{GS}/I_{G} \)

\( V_{GS} = 1.5 \text{ V} \)
\( V_{GS} = 0.5 \text{ V} \)

\( V_{DS} \) (V)

NMOS, \( t_{ox} = 2 \text{ nm}, W/L = 10/0.6 \mu \text{m} \)

Physical background: Outline

- Introduction
- DC-Model
- AC-Model
- Noise Model
- Summary
AC-Model: intrinsic charges

\[ Q_s = W \cdot \int_0^L \left(1 - \frac{x}{L}\right) \cdot Q_{\text{inv}} \cdot dx \]

\[ Q_G = -Q_D - Q_S - Q_B \]

\[ Q_o = W \cdot \int_0^L x \cdot Q_{\text{inv}} \cdot dx \]

Intrinsic Capacitances:

\[ C_{ij} = \begin{cases} \frac{\partial Q_i}{\partial V_j} & \text{for } i = j \\ -\frac{\partial Q_i}{\partial V_j} & \text{for } i \neq j \end{cases} \]

where \( i, j = G, S, D \) or \( B \)

AC-Model: input capacitance \( C_{gg} \)

\( (V_{DS} = 0 \text{ V}, W/L = 80*612/2.5\mu \text{m}) \)

\( \begin{array}{c|c|c}
\text{NMOS} & \text{CMOS18} & \text{PMOS} \\
\hline
V_{GS} (V) & C_{gg} (nF) & C_{gg} (nF) & C_{gg} (nF) \\
\hline
\end{array} \)

\( V_{GS} \) values range from -3 to 3.

Measurements indicated by markers.
MOS Model 9 ($V_{DS}=0\,V$, $W/L=80\times612/2.5\mu m$)

**AC-Model: input capacitance $C_{gg}$ (MM9)**

![Graph showing $C_{gg}$ vs $V_{DS}$ for NMOS and CMOS18, with poly-depletion markers.]

- **NMOS**
  - $V_{DS}$ (V)
  - $C_{gg}$ (nF)
  - Measurements
  - MOS Model 9
  - $t_{ox} = 3.8\,nm$

- **CMOS18**
  - $V_{DS}$ (V)
  - $C_{gg}$ (nF)
  - Measurements
  - MOS Model 9
  - $t_{ox} = 4.3\,nm$

**AC-Model: accumulation**

- $V_{GB} < V_{FB}$

![Graph showing $\psi_s$ vs $V_{GB} - V_{FB}$ for accumulation, weak-inversion, and strong-inversion regions.]

- $t_{ox} = 3.2\,nm$
- $N_A = 2\times10^{17}\,cm^{-3}$
- $V = 0\,V$
- $q\cdot \psi_s$
- $q\cdot \phi_F$
AC-Model: input capacitance \( C_{\text{GG}} \) (\( \psi_s \)-based model)

\( \psi_s \)-based model (PMOS, \( V_{\text{DS}} = 0 \) V, \( W/L = 80\times612/2.5 \mu \text{m} \))

Poly-depletion effect

Depletion layer formed in gate resulting in effective gate potential:

\[
V_{\text{GB}} - V_{\text{FB}} - \psi_s - \psi_p
\]

Body factor of poly-silicon:

\[
k_p = \frac{\sqrt{2 \cdot q \cdot \varepsilon_{\text{Si}} \cdot N_p}}{C_{\text{ox}}}
\]
AC-Model: poly-depletion effect

influence of poly-depletion ($V_{DS}=50\text{mV}$, $V_{SB}=0\text{V}$)

- $k_p \rightarrow \infty$
- $k_p = 2$

$V_L = 10/10\mu\text{m}$

- Drain current
- Gate capacitance

AC-Model: poly-depletion effect

- 0.18$\mu\text{m}$ CMOS
- $W/L = 80*612/2.5\mu\text{m}$

- NMOS: $t_{ox} = 3.6\text{nm}$
- PMOS: $t_{ox} = 3.2\text{nm}$
AC-Model: quantum-mechanical effects

- energy quantization
- charge centroid

\[
\begin{align*}
\Delta E & \\
E_C & \\
E_F & \\
E_i & \\
E_V & 
\end{align*}
\]

\[
\text{Gate} \quad \text{Oxide} \quad \text{Substrate}
\]

⇒ results in \( \Delta V_T \)

⇒ results in \( \Delta t_{ox} \)

inversion-layer is formed at distance \( \Delta y \) from interface

\[
\Delta y \propto E_{\text{eff}}^{-1/6}
\]


effective oxide thickness:

\[
t_{ox_{\text{eff}}} = t_{ox} + \frac{e_{ox}}{e_{\text{Si}}} \cdot \Delta y
\]
AC-Model: quantum-mechanical effects

NMOS 0.18μm CMOS
W/L=80*612/2.5μm
using physical $t_{ox}=3.2$nm

AC-Model: reciprocity of capacitances

reciprocity: at $V_{DS}=0$ V one should have $C_{ij}=C_{ji}$

$C_{DS}-C_{SD}$ vs. $V_G$

MM11 shows almost perfect reciprocity (better than 0.01 $C_{ox}$)
AC-Model: symmetry of capacitances

symmetry: at $V_{DS}=0$ V one should have $C_{ID}=C_{IS}$

$C_{BD}-C_{BS}$ vs. $V_G$

MM11 shows perfect symmetry

AC-Model: bias-dependent overlap capacitance

Two-terminal MOS-capacitance: accumulation and depletion region included

introducing two parameters: $k_{ov}$ and $V_{FBov}$
AC-Model: bias-dependent overlap capacitance

PMOS, $V_{DS}=0$ V, $W/L=152\times612/0.18\mu$m

![Graph showing the relationship between $C_{DG}$ and $V_{GS}$ for PMOS with $V_{DS}=0$ V. The graph includes measurements and models showing total and intrinsic overlap capacitance.]

Physical background: outline

- Introduction
- DC-Model
- AC-Model
- Noise Model
- Summary
Noise Model: definitions

- **input-referred noise:**
  \[ S_d = \frac{\langle (I_d(t) - I_d)^2 \rangle}{\Delta f} \]

- **noise figure:**
  \[ F = 1 + \frac{S_{V_{in}}}{S_{V_{out}}} \]
  \[ S_{V_{input}} = 4kT \cdot R_S \]
**Noise Model: noise types in MOS transistor**

- 1/f noise
- Thermal noise

**Noise Model: 1/f-noise**

- Number of carriers in inversion channel fluctuates
- Mobility also fluctuates
- Correlation

Noise Model: 1/f-noise (II)

- single trap: Random Telegraph Signals (RTS)
- leads to Lorentzian noise spectrum
- this is indeed observed in small-area devices

Noise Model: 1/f-noise (III)

- uniform distribution trapping distances
- distribution of traps leads to 1/f spectrum
Noise Model: 1/f-noise (IV)

• unified 1/f noise model: BSIM4, MM9 & MM11
• bias dependence verified
• geometrical scaling verified

Noise Model: thermal noise

• thermal noise: due to the random thermal motion of charge carriers

• Nyquist’s law for a resistor:

\[ S_l = \frac{4 \cdot k_B \cdot T}{R} \]

\[ S_V = 4 \cdot k_B \cdot T \cdot R \]
**Noise Model: thermal noise (II)**

\[ I_D = g(x) \frac{dV}{dx} \]

\[ g(x) = W \cdot \mu(x) \cdot Q_{inv}(x) \]

\[ \Rightarrow \Delta I_D = -\frac{g(x)}{L} \cdot \Delta V \]

**Nyquist's law:**

\[ S_{AV} = \frac{4 \cdot k_B \cdot T}{g(x)} \]

\[ \Rightarrow S_{ID} = \frac{4 \cdot k_B \cdot T}{I_D \cdot L^2} \cdot \int_{0}^{V_{D(SAT)}} g^2(V) \, dV \]


---

**Noise Model: thermal noise (III)**

- **thermal noise:**

\[ S_{ID} = \frac{4 \cdot k_B \cdot T}{I_D \cdot L^2} \cdot \int_{0}^{V_{D(SAT)}} g^2(V) \, dV \]

where: \( g(V) = -W \cdot \mu(V) \cdot Q_{inv}(V) \)


**Old expression (BSIM.MM9) vs. New expression (MM11):**

<table>
<thead>
<tr>
<th>Old expression</th>
<th>New expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>[ \mu = \frac{\mu_{eff}}{1 + \frac{\mu_{eff}}{V_{Sat} \cdot E_{</td>
<td></td>
</tr>
</tbody>
</table>
Noise Model: thermal noise (IV)

50Ω Noise Figure (NMOS, W/L=160/0.35μm, $V_{DS}=3.3V$)

$F_{dB}$ (dB)

$V_{GS}$ (V)

no hot electron effect needed to describe noise behaviour


Noise Model: thermal noise (V)

50Ω noise figure (no noise parameters needed)

$F_{dB}$ (dB)

$V_{gs}$ (Volts)

verified on 0.35μm, 0.25μm and 0.18μm CMOS

Summary

MOS Model 11, fulfills demands for advanced compact MOS modelling:
- use of $\psi_s$-formulations results in accurate description of moderate inversion region
- improved description of several physical effects results in accurate and symmetrical description of currents, charges, noise and distortion
- fulfills Compact Model Council benchmark tests
- parameters determined from $I$-$V$ and $C$-$V$ measurements
- no increase in number of parameters
- no increase in simulation time
- verified on 100nm CMOS technology and sub-100nm devices
- no Gate-Induced Drain Leakage (GIDL) implemented yet

Availability

- public domain
  - source code in C (including solver)
  - documentation of model and parameter extraction
  - http://www.semiconductors.philips.com/Philips_Models
- circuit simulators
  - Pstar (Philips in-house)
  - Spectre (Cadence)
  - Hspice (Avant!)
  - ADS (Agilent)
  - Eldo (Mentor Graphics)
  - HSIM (NASSDA)
Appendices

- Accuracy of $\psi_s$-approximation
- Linear/saturation region transition

Appendix: accuracy of surface potential approximation

```
absolute error in $\psi_s$  $\rightarrow$ relative error in $I_{DS}$
```

$\Rightarrow$ error in $I_{DS}$ due to $\Delta\psi_s$ error is negligible
Appendix: linear/saturation transition

Model incorporates linear/saturation region for long-channel case:

\[ V_{DSAT} = V_{DSAT_{long}} \]

\[ \Rightarrow \text{Short-channel devices: } V_{DSAT} < V_{DSAT_{long}} \]

Approximation used:

\[ \psi_s = \psi_s (V_{GB}, V_{DSx} + V_{SB}) \]

where:

\[ V_{DSx} = \frac{V_D S \cdot V_{DSAT}}{(V_{DS}^{2m} + V_{DSAT}^{2m})^{\frac{1}{2m}}} \]


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Literature

- “Accurate thermal noise model for deep sub-micron CMOS”, A.J. Scholten et al., IEDM'99 Technical Digest, p.155, 1999
Literature

- “RF-Distortion characterisation of sub-micron CMOS”,
- “RF-Distortion in deep sub-micron CMOS technologies”,
  R. v. Langevelde et al., IEDM’00 Technical Digest, p.807, 2000
- “BSIM4 and MOS Model 11 benchmarks for MOSFET capacitances”,
- “MOS Model 11, Level 1100”, R. v. Langevelde,
  Nat.Lab. Unclassified Report NL-UR 2001/813, April 2001, see website
- “Compact modelling of pocket-implanted MOSFETs”,
- “Gate current: Modeling, ΔL extraction and impact on RF performance”,
  R. v. Langevelde et al., IEDM’01 Technical Digest, p.289, 2001
- “Parameter extraction for surface-potential based compact MOS Model 11”,
- “MOS Model 11, Level 1101”, R. v. Langevelde et al.,
Introduction: MOS Model 11

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- suitable for digital, analog and RF
- suitable for modern/future CMOS processes
- physics based
- simulation time comparable to MM9
- number of parameters comparable to MM9
- simple parameter extraction
Introduction: parameter extraction

IC-CAP used for parameter extraction

interface with circuit simulator:

IC-CAP → IC-CAP to Pstar interface → Pstar circuit simulator

DC CV

MOS Model 11

Introduction: structure of MOS Model 11

\[ W, L \]

Geometry Scaling

\[ T \]

Temperature Scaling

\[ V_{SB}, V_{GS}, V_{DS} \]

Model Equations

Junction diodes modelled by separate model

Currents
Charges
Noise

Let's make things better

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Introduction: parameter structure

\[ k_{OR} + S_L \cdot \left( \frac{1}{L_E} - \frac{1}{L_R} \right) + S_{L^2} \cdot \left( \frac{1}{L_E^2} - \frac{1}{L_R^2} \right) + S_W \cdot \left( \frac{1}{W_E} - \frac{1}{W_R} \right) = k_O \]

Introduction: parameter extraction strategy

- measurements
- extract miniset for each cut
- determine temperature scaling
- determine geometry scaling
- parameter set

example: 0.12μm CMOS
Parameter extraction: outline

- Measurements
- Miniset extraction
- Temperature scaling
- Geometry scaling

Measurements: set-up

IC-CAP used for measurements:

![Diagram showing measurement setup]
9MOS Model 11: Parameter Extraction

**Measurements: DC parameters**

**required measurements per device (NMOS)**

<table>
<thead>
<tr>
<th></th>
<th>output</th>
<th>1st-order sweep</th>
<th>2nd-order sweep</th>
<th>constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$I_D$, $g_m$</td>
<td>$V_{GS}=0 \rightarrow V_{DD}$</td>
<td>$V_{SB}=0 \rightarrow V_{DD}$</td>
<td>$V_{DS}=50$ mV</td>
</tr>
<tr>
<td>2</td>
<td>$I_D$, $g_{DS}$</td>
<td>$V_{DS}=0 \rightarrow V_{DD}$</td>
<td>$V_{GS}=V_T \rightarrow V_{DD}$</td>
<td>$V_{SB}=0$ V</td>
</tr>
<tr>
<td>3</td>
<td>$I_D$, $I_G$, $I_B$</td>
<td>$V_{GS}=-V_{DD} \rightarrow V_{DD}$</td>
<td>$V_{DS}=0 \rightarrow V_{DD}$</td>
<td>$V_{SB}=0$ V</td>
</tr>
<tr>
<td>4</td>
<td>$C_{GG}$</td>
<td>$V_{GS}=-V_{DD} \rightarrow V_{DD}$</td>
<td>-----</td>
<td>$V_{DS}=V_{SB}=0$ V</td>
</tr>
</tbody>
</table>

**Measurements: DC parameters (II)**

**required measurements per device (NMOS)**

1. $I_D$ - $V_{GS}$ - curve for various $V_{SB}$ in linear region
2. $I_D$ - $V_{DS}$ - and $g_{DS}$ - $V_{DS}$ - curves for various $V_{GS}$
3. $I_G$ - $V_{GS}$ - and $I_B$ - $V_{GS}$ - curves for various $V_{DS}$
4. $C_{GG}$ - $V_{GS}$ - curve at $V_{SB}=V_{DS}=0$ V
Measurements: AC parameters

required capacitance measurements

$$C_{CG} - V_{GS} \quad C_{BG} - V_{GS} \quad C_{GG} - V_{GS}$$

$$C_{GG} = C_{CG} + C_{BG} \quad \Rightarrow \quad C_{GG} \text{ is redundant}$$

Parameter extraction: outline

- Measurements
- Miniset extraction
  - DC parameters
  - AC parameters
- Temperature scaling
- Geometry scaling
### Miniset extraction: DC-model parameters

<table>
<thead>
<tr>
<th>effect</th>
<th>parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>threshold</td>
<td>$k_o, \varphi_B$</td>
</tr>
<tr>
<td>subthreshold slope</td>
<td>$m_o$</td>
</tr>
<tr>
<td>flat-band voltage</td>
<td>$V_{FB}$</td>
</tr>
<tr>
<td>poly depletion</td>
<td>$k_p$</td>
</tr>
<tr>
<td>mobility reduction</td>
<td>$\beta, \theta_{sr}, \theta_{ph}, \eta_{mob}$</td>
</tr>
<tr>
<td>series resistance</td>
<td>$\beta, \theta_R$</td>
</tr>
<tr>
<td>velocity saturation</td>
<td>$\theta_{sat}$</td>
</tr>
<tr>
<td>conductance</td>
<td>$\alpha, \sigma_{DIBL}, \sigma_{sf}, \theta_{Th}$</td>
</tr>
<tr>
<td>impact ionization</td>
<td>$a_1, a_2, a_3$</td>
</tr>
<tr>
<td>gate current</td>
<td>$I_{INV}, B_{INV}, I_{GACC}, B_{ACC}, I_{GOV}$</td>
</tr>
</tbody>
</table>

### Miniset extraction: threshold voltage

Threshold voltage $V_{TO}$ can be calculated by:

$$V_{TO} = V_{FB} + \psi_o + \left(\frac{k_o}{k_p}\right)^2 \cdot \psi_o + k_o \cdot \sqrt[3]{\psi_o}$$

where:

$$\psi_o = \varphi_B + 2 \cdot \frac{k_B \cdot T}{q}$$

Neglecting the poly-depletion effect:

$$V_{TO} = V_{FB} + \psi_o + k_o \cdot \sqrt[3]{\psi_o}$$
Miniset extraction: strategy

**extraction strategy:**
- 1st-order estimation
- (optional) flat-band voltage/poly depletion
- somewhat different strategy for long-channel and short-channel devices
- (sub)threshold parameters
- mobility/series-resistance
- velocity saturation/conductance
- start with long-channel device
- gate current
- impact ionization

Miniset extraction: long-channel device

**Step 1: 1st-order estimation**

![Diagram showing 1st-order parameter estimation with symbols and parameters](image)

- doping concentration in polysilicon gate
- $t_{ox}$, $N_P$
- $W$, $L$
- 1st-order parameter estimate
- miniset parameters
Miniset extraction: long-channel device

**Step 1: 1st-order estimation**

optimize $I_D$ and $g_m$ on absolute error: $\phi_B$, $k_o$, $\beta$ and $\theta_{sr}$

**Threshold**

**Mobility**

![Graphs showing $I_D$ and $g_m$ vs. $V_{GS}$ for NMOS](image)

$W/L = 10/10 \mu m$
Miniset extraction: long-channel device

Step 2: $V_{FB}$/poly-depletion (optional)

optimize $C_{GG}$ on relative error: $V_{FB}$, $\phi_B$, $k_0$ and $1/k_p$

poly-depletion

measurement error due to gate current

NMOS

$W/L=100/10\mu m$
Miniset extraction: long-channel device

**Step 3: subthreshold parameters**

optimize $I_D$ on relative error: $\phi_B$, $k_o$ and $m_o$

![Graph showing subthreshold parameters](image)

**Normos $W/L=10/10\mu m$**

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Miniset extraction: long-channel device

**Step 4: mobility parameters**

- Optimize $I_D$ and $g_m$ on relative error: $\beta$, $\theta_{sr}$, $\theta_{ph}$ and $\eta_{mob}$

- Mobility reduction

** NMOS W/L=10/10µm **
Miniset extraction: long-channel device

**Step 5: velocity saturation/conductance**

- Optimize $I_D$ on absolute error: $\theta_{\text{sat}}$
- Optimize $g_{DS}$ on relative error: $\alpha$, $\sigma_{sf}$ and $\theta_{\text{th}}$

![Graphs showing $I_D$ and $g_{DS}$ vs $V_{DS}$ for NMOS with $W/L=10/10\mu m$](image)
Miniset extraction: long-channel device

Step 6: gate current parameters
optimize $I_G$ on absolute error: $B_{inv}$ and $I_{GINV}$

gate-to-channel current

Miniset extraction: long-channel device

Step 6: gate current parameters
optimize $I_G$ on relative error: $I_{GACC}$ and $I_{GOV}$

gate-bulk & overlap current
Miniset extraction: long-channel device

Step 6: gate current parameters
optimize $I_G$ on relative error: $I_{GAC}$ and $I_{GOV}$

gate-bulk & overlap current

Miniset extraction: long-channel device

Repeat steps 3 through 6, e.g. step 4:
optimize $I_D$ and $g_m$ on relative error: $\beta$, $\theta_{sr}$, $\theta_{ph}$ and $\eta_{mob}$

error due to gate current
Miniset extraction: long-channel device

Repeat steps 3 through 6, e.g., step 4:
optimize $I_D$ and $g_m$ on relative error: $\beta$, $\theta_{sr}$, $\theta_{ph}$ and $\eta_{mob}$

![Graphs showing $I_D$ and $g_m$ vs. $V_{GS}$ for NMOS with $W/L=10/10\mu m$](image)

Miniset extraction: short-channel device

**Step 1: 1st-order estimation**

copy $V_{FB}$, poly-depletion, mobility reduction and tunnelling probability ($B_{in,w}$) parameters from long-channel device; other parameters are estimated:

$W$, $L$  
$\rightarrow$  
$1^{st}$-order parameter estimate  
$\rightarrow$  
miniset parameters

$\rightarrow$  
$t_{ox}$
Miniset extraction: short-channel device

**Step 1: 1st-order estimation**

Optimize $I_D$ and $g_m$ on absolute error: $\phi_B$, $k_0$, $\beta$ and $\theta_R$

Threshold $R_{series}$

![I-D and g-m graphs](image)

NMOS $W/L=10/0.12\mu m$
Miniset extraction: short-channel device

**Step 2: subthreshold parameters**

Optimize \( I_D \) on relative error: \( \phi_B \), \( k_o \) and \( m_o \)

NMOS \( W/L=10/0.12\mu m \)

**Subthreshold slope**

**Optimization region**

**Graphical representation**

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Miniset extraction: short-channel device

Step 3: series-resistance
optimize $I_D$ and $g_m$ on relative error: $\beta$ and $\theta_R$

$R_{\text{series}}$

$I_D$ (mA)

$g_m$ (µA/V)

Optimization region

NMOS $W/L=10/0.12\mu m$

$V_{GS}$ (V)

$V_{GS}$ (V)
Miniset extraction: short-channel device

Step 4: velocity saturation/conductance
- Optimize $I_D$ on absolute error: $\theta_{sat}$
- Optimize $g_{DS}$ on relative error: $\alpha$, $\sigma_{sf}$, $\sigma_{DIBL}$, and $\theta_{Th}$

![Graphs showing $I_D$ and $g_{DS}$ vs. $V_{DS}$ for NMOS devices with W/L=10/0.12μm]
Miniset extraction: short-channel device

Step 5: gate current parameters
optimize $I_G$ on relative error: $I_{GAC}$, $I_{GOV}$ and $I_{GINV}$

gate current

NMOS
$W/L=10/0.12\mu m$

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Parameter extraction: outline

- Measurements
- Miniset extraction
  - DC parameters
  - AC parameters
- Temperature scaling
- Geometry scaling

Miniset extraction: AC : short-channel device

Step 1: oxide capacitance $C_{OX}$

Optimize $C_{BG}$ on relative error: $C_{OX}$

![Graph showing $C_{BG}$ vs. $V_{GS}$ for NMOS with $W/L=100/0.13\mu m$]
Miniset extraction: AC : short-channel device

**Step 1: oxide capacitance** $C_{OX}$

- Optimize $C_{BG}$ on relative error: $C_{OX}$

![Graph showing $C_{BG}$ as a function of $V_{GS}$ for a NMOS with $W/L=100/0.13 \mu m$.]

**Step 2: overlap capacitance**

- Optimize $C_{CG}$ on relative error: $C_{GSO}$, $k_{ov}$ and $V_{FBoV}$

$C_{GSO} = C_{GDO}$

![Graph showing $C_{CG}$ as a function of $V_{GS}$ for a NMOS with $W/L=100/0.13 \mu m$.]
Parameter extraction: outline

- Measurements
- Miniset extraction
- Temperature scaling
- Geometry scaling
Temperature scaling: introduction

Temperature scaling rules of the form:

\[ \beta_T = \beta \left( \frac{T_R}{T} \right)^{n_B} \quad \text{or} \quad \varphi_{BT} = \varphi_B + S_{T,IB} \left( T - T_R \right) \]

where \( T_R \) is room temperature

Miniset parameters at room temperature are exactly reproduced

Temperature scaling: strategy

Extraction strategy:

- 1st-order estimation
- (sub)threshold parameters
- Mobility/series-resistance
- Velocity saturation
- Impact ionization

Somewhat different strategy for long-channel and short-channel devices

⇒ Start extraction for long-channel device

(Use default values of temperature parameters as 1st-order estimation)
Step 1: subthreshold parameters
optimize $I_D$ on relative error: $S_{T,Vfb}$

NMOS $W/L = 10/10 \mu m$
Temperature scaling: long-channel device

Step 2: mobility parameters
optimize $I_D$ on relative error: $\eta_p$, $\eta_s$, and $\eta_h$

$T=125^\circ C$

$T=-40^\circ C$

$W/L=10/10\,\mu m$

\[ \begin{align*}
I_D (\mu A) & \\
0 & 5 & 10 & 15 & 20 & 25 \\
0.0 & 0.4 & 0.8 & 1.2 \\
V_{GS} (V) & \\
\end{align*} \]
Temperature scaling: long-channel device

**Step 3: velocity saturation**

optimize $I_D$ on relative error: $\eta_{sat}$

$T=125^\circ C$

$T=-40^\circ C$

$V_{DS} (V)$

$W/L=10/10\mu m$

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Temperature scaling: short-channel device

**Step 1: 1st-order estimation**
copy temperature scaling parameter values from long-channel device

Temperature scaling: short-channel device

**Step 2: subthreshold parameters**
optimize \( I_D \) on relative error: \( S_{T=125^\circ C} \)

\( T=125^\circ C \) no fit needed

\( T=-40^\circ C \)

\( I_D \) (A) vs. \( V_{GS} \) (V)

NMOS
\( W/L=10/0.12 \) \( \mu \)m
Temperature scaling: short-channel device

**Step 3: series-resistance**

optimize $I_D$ on relative error: $\eta_R$ and $\eta_R$

$T=125^\circ C$

$T=40^\circ C$

$W/L=10/0.12\mu m$

NMOS

Let's make things better
Temperature scaling: short-channel device

**Step 4: velocity saturation**

optimize $I_D$ on relative error: $\eta_{\text{sat}}$

![Graphs showing $I_D$ vs. $V_{DS}$ at different temperatures](image)

**Notes:**
- $V_{DS}$
- $T=125^\circ C$
- $T=-40^\circ C$
- NMOS $W/L=10/0.12\mu m$
Parameter extraction: outline

- Measurements
- Miniset extraction
- Temperature scaling
  - Geometry scaling

Geometry scaling: $\Delta L$ and $\Delta W$ extraction

$$L_E = L_{\text{drawn}} - \Delta L$$
$$W_E = W_{\text{drawn}} - \Delta W$$

- conventional extraction uses gain factor: $\beta \propto \frac{W_E}{L_E}$

$\Delta L$ extraction fails for pocket implanted devices
**Geometry scaling: ΔL extraction**

- **use** $C_{GB}$ **in accumulation** (A. Scholten et al, Essderc’01)
- **use** gate current, e.g. $I_{GInv}$ vs. $L_{drawn}$: $I_{GInv} \propto L_E \cdot W_E$

![Graph showing $I_{GInv}$ vs. $L_{drawn}$ for PMOS with $W = 10 \mu m$](image)

**Geometry scaling: scaling rules**

Two types of geometry scaling rules can be used:

- **Binning scaling rules**
  - fast and easy, however not physical
  - reproduces minisets
  - use 170 parameters per bin

- **Physical scaling rules**
  - somewhat more elaborate, but physical
  - gives insight in technology
  - use 90 parameters per technology
Geometry scaling: binning scaling rules

- binning rules based on physical scaling
- no parameter jumps at bin borders
- minisets are exactly reproduced at corners

⇒ binning parameter set is calculated from minisets
⇒ no extra extraction or optimization needed

Geometry scaling: physical scaling rules

Physical scaling rules have different forms per miniset parameter, e.g.:

\[
k_0 = k_0 \beta^2 \left[ 1 + \frac{S_{L1} k_0}{L_E} + \frac{S_{L2}^2 k_0}{L_E^2} \right] \left[ 1 + \frac{S_{W1} k_0}{W_E} \right]
\]

or:

\[
\beta = \frac{\beta_{sq}}{1 + f_{\beta} \frac{L_p}{L_E} \left[ 1 - \exp \left( - \frac{L_p}{L_E} \right) \right]} \cdot \frac{W_E}{L_E}
\]

Scaling parameters determined from miniset values

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Geometry scaling: body factor $k_0$

scaling of body factor $k_0$

$W = 10\mu m$
NMOS

MM11 scaling rule

miniset values

$L_{drawn}$ (\(\mu m\))

$W = 10\mu m$
PMOS

$1/\beta$ (KV/\(A\))

MM11 scaling rule

conventional scaling rule

conventional scaling: $\beta = \beta_{sv} \cdot \frac{W_E}{L_E}$
Geometry scaling: \( I_D-V_{GS} \)-curves

Physical geometry scaling fits of linear region (PMOS)

\[
\begin{align*}
\text{WIL} &= 10/10\mu m & \text{WIL} &= 10/0.8\mu m & \text{WIL} &= 10/0.12\mu m
\end{align*}
\]

Geometry scaling: \( g_m-V_{GS} \)-curves

Physical geometry scaling fits of linear region (PMOS)

\[
\begin{align*}
\text{WIL} &= 10/10\mu m & \text{WIL} &= 10/0.8\mu m & \text{WIL} &= 10/0.12\mu m
\end{align*}
\]
**Geometry scaling: subthreshold curves**

Physical geometry scaling fits of subthreshold region (PMOS)

![Graphs showing I_D vs V_GS for different W/L ratios](image)

**W/L = 10/10 μm**  
**W/L = 10/0.8 μm**  
**W/L = 10/0.12 μm**

---

**Geometry scaling: I_D-V_DS-curves**

Physical geometry scaling fits of output curves (PMOS)

![Graphs showing I_D vs V_DS for different W/L ratios](image)

**W/L = 10/10 μm**  
**W/L = 10/0.8 μm**  
**W/L = 10/0.12 μm**
Geometry scaling: \( g_{DS} - V_{DS} \)-curves

physical geometry scaling fits of output curves (PMOS)

\[ W/L = 10/10 \mu m \quad W/L = 10/0.8 \mu m \quad W/L = 10/0.12 \mu m \]

Geometry scaling: \( I_G - V_{GS} \)-curves

physical geometry scaling fits of gate current (PMOS)

\[ W/L = 10/10 \mu m \quad W/L = 10/0.8 \mu m \quad W/L = 10/0.12 \mu m \]
Conclusions

MOS Model 11 is a symmetric, $\psi_s$-based model:

- Its parameter extraction is simple, and only uses DC and CV measurements.
- Temperature scaling is implemented on miniset-level (in contrast to MM9).
- It has a choice between two geometry scaling rules: binning and physical rules.
- www.semiconductors.philips.com/philips_models