RF-CMOS Performance Trends

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***Abstract*—The impact of scaling on the analog performance of MOS devices at RF frequencies was studied. Trends in the RF performance of nominal gate length NMOS devices from 350-nm to 50-nm CMOS technologies are presented. Both experimental data and circuit simulations with an advanced validated compact model (MOS Model 11) have been used to evaluate the RF performance. RF performance metrics such as the cutoff frequency, maximum oscillation frequency, power gain, noise figure, linearity, and $1/f$ noise were included in the analysis. The focus of the study was on gate and drain bias conditions relevant for RF circuit design. A scaling methodology for RF-CMOS based on limited linearity degradation is proposed.**

***Index Terms*—CMOS integrated circuits, MOS devices, modeling, radio frequency.**

I. Introduction

THE scaling of CMOS has resulted in a strong improvement in the RF performance of MOS devices [1], [2], [15]. Consequently, CMOS has become a viable option for analog RF applications and RF system-on-chip. Performance metrics such as cutoff frequency, maximum oscillation frequency, and minimum noise figure have been studied widely [1], [2], [8]. However, trends in large signal performance (linearity) and low-frequency noise are not well known. Linearity and noise are key parameters for RF circuits such as low-noise amplifiers (LNAs). Low-frequency noise is important for the phase noise of RF circuits such as voltage-controlled oscillators (VCOs). Phase noise and linearity specifications are severe for future wide-band communication systems.

The emphasis of previous work [1], [8] was on the maximum or minimum values of the RF parameters, i.e., power consumption was neglected. However, for circuit applications, the RF performance at low gate bias (i.e., just above threshold) is more important. Trends in the RF performance, $1/f$ noise, and linearity at such bias conditions are not well known. First-order equations for the RF figures of merit (FOM) are not suited to predict the RF performance at arbitrary bias conditions. Instead, a more appropriate method would be to use circuit simulation with a validated compact model. A detailed study of the key RF performance metrics including noise and linearity at bias conditions which are relevant for RF circuit design is needed.

In this paper, the RF performance of nominal gate length NMOS devices from 350-nm to 50-nm CMOS technologies is studied at bias conditions relevant for RF design (i.e., saturation conditions and gate bias near threshold). Experimental results including RF FOM such as the cutoff frequency (f_t), maximum oscillation frequency (f_max), maximum stable gain (g_msg), minimum noise figure ($\mathrm{NF_{min}}$), linearity (V_IP3), and $1/f$ noise level are presented for three industrial CMOS technologies with feature sizes of 350 nm, 250 nm, and 180 nm. Circuit and device simulation results for the RF device performance are presented for nominal gate length NMOS devices from CMOS technologies with feature size down to 50 nm. A validated compact model (MOS Model 11) [3], [5], [6] is used for prediction of the RF performance trends. This model has been especially developed to give an accurate description of the linearity. It is well suited for digital, analog, and RF simulation. In Section VII, a scaling methodology for RF-CMOS for limited linearity degradation is presented.

II. RF Figures of Merit

First-order equations for the RF FOM such as the cutoff frequency f_t, the maximum oscillation frequency f_max based on the maximum available gain (MAG), minimum noise figure $\mathrm{NF_{min}}$, and third harmonic intercept voltage V_IP3 are given below [4]

$$f_\mathrm{t} = \frac{1}{2\pi} \cdot \frac{g_\mathrm{m}}{C_\mathrm{gg} + C_\mathrm{par} + C_\mathrm{gso} + C_\mathrm{gdo}} \tag{1}$$

$$f_\mathrm{max} = \frac{f_\mathrm{t}}{2\sqrt{(R_\mathrm{g} + R_\mathrm{i})(g_\mathrm{ds} + 2\pi f_\mathrm{t} C_\mathrm{gdo})}} \tag{2}$$

$$NF_\mathrm{min} = 1 + K \cdot \frac{f}{f_\mathrm{t}} \sqrt{g_\mathrm{m}(R_\mathrm{g} + R_\mathrm{i} + R_\mathrm{s})} \tag{3}$$

$$V_\mathrm{IP3} = \sqrt{\frac{24 \cdot g_\mathrm{m}}{g_\mathrm{m3}}} \tag{4}$$

where g_m is the transconductance; g_m3 is the third-order derivative of the drain current versus gate bias; and V_IP3 is the extrapolated input voltage amplitude at which the first- and third-order output amplitudes are equal. The capacitances C_gg, C_par, C_gso, and C_gdo are the intrinsic input capacitance, parasitic gate-bulk capacitance, and the gate-source and gate-drain overlap capacitances. R_g is the gate resistance and R_i is the real part of the input impedance due to nonquasistatic effects. R_s and g_ds are the source series resistance and output conductance. The above equations give an indication of the impact of technology parameters on the RF FOM. For linearity FOM V_IP3 is used as a first-order parameter, a large V_IP3 is required for high linearity. V_IP3 is easily obtained from the dc characteristics. It gives a good indication of the device linearity even at high frequency

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[11]. Note that f_t, f_{max}, and NF_{min} are obtained at different measurement and impedance matching conditions. This has to be taken into account in the analysis. The parameters f_{max} and NF_{min} are only slightly affected by parasitic capacitance at the input (i.e., as long as its quality factor is high). For this reason, the influence of parasitic gate-bulk capacitance is not taken into account in the analysis of the cutoff frequency, noise figures, and f_{max}.

III. Experimental Details

The minimum gate length NMOS devices from 350-nm, 250-nm, and 180-nm mainline CMOS technologies were studied. The wafers were supplied by industrial foundries. The device width was varied between 160 and 192 μm. An optimized multi-finger layout (common source type) with five to six layers of metal was used to reduce parasitics (R_g, R_b, C_{jun}). The finger width was varied between 2.5 and 160 μm. Small-signal S-parameters were measured on wafer up to 40 GHz using a HP8510 Network Analyzer.

Linearity (V_{IP3}) was measured by a dc method. Very high accuracy current–voltage (I–V) characteristics were obtained using Keithley 2400 SourceMeters. The higher order transconductances were obtained by numerical differentiation.

Low frequency noise was measured on packaged devices. NMOS and PMOS transistors (with $W \times L = 10 \times 4\ \mu m^2$, where W and L are the transistor width and length, respectively) were dc characterized before noise measurement. From every variant, three to four nominally identical samples (with minimal dc parameter variation) were selected for $1/f$ noise measurements. Noise measurements were all performed under saturation conditions and at variable effective gate bias V_{gt} ($= V_{gs} - V_t$ where V_t is the threshold voltage). They were carried out with a BTA 9812A standard noise probe. We present data in terms of S_{vgate}, the input referred voltage spectral density, which is defined as: $S_{vgate} \equiv S_I/g_m^2$, with g_m the transconductance. Average S_{vgate} values at 100 Hz and standard deviations based on sample-to-sample spread were determined. The sample-to-sample spread is at most a factor of 2. RF noise was measured on wafer up to 15 GHz using a HP8790U noise figure measurement system. Details will be published elsewhere.

For accurate RF simulations MOS model 11 [3] with junction capacitance, substrate and gate resistance [6], and high-frequency noise model [5] was used. The model was validated previously for these technologies. This model has been especially developed to give an accurate description of the linearity. MOS Model 11 includes gate depletion and quantum mechanical corrections to the gate capacitance. The model of Hung *et al.* [12] is included for $1/f$ noise modeling. For the simulations a device width of 192 μm was used. This width is typical for an LNA amplifier. A folded layout was used; the finger width was scaled in proportion with the technology. The data are plotted versus drain current per micron device width for the maximum allowed drain bias. This is more relevant for power constrained scaling. Note that there is a direct relation between the drain current and the applied gate bias.

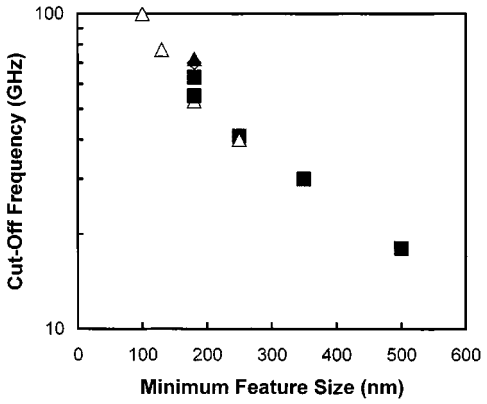

Fig. 1. Measured f_t data of nominal gate length NMOS devices from industrial CMOS technologies versus minimum feature size. (■: Philips, △ [1], ▲ [2], ◇ [8]).

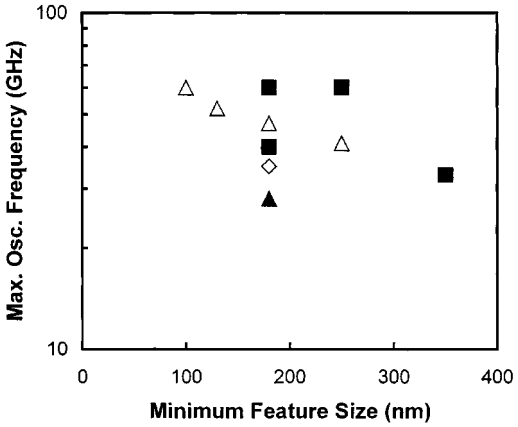

Fig. 2. f_{max} data of nominal gate length NMOS devices versus minimum feature size (■ Philips data, △ [1], ▲ [2], ◇ [8]).

IV. Experiments

The measured maximum f_t of 350-nm, 250-nm, and 180-nm NMOS devices is plotted in Fig. 1 with data from [1], [2], and [8]. The total device width was either 160 μm or 192 μm. For the 180-nm technology f_t exceeds 60 GHz. A strong improvement with scaling is observed due to an increased g_m. Our data are in line with those from references [1], [2], and [8]. In Fig. 2, f_{max} values (based on MAG extrapolation) of nominal devices are plotted together with data from [1], [2], and [8]. Our data exceed 50 GHz for both 250-nm and 180-nm devices. It should be noted that the measurement of f_{max} is difficult. Extrapolation of g_{max} (maximum available gain) above the range of the measurement frequency is a challenge. Hence, the accuracy of the f_{max} data is limited. The values reported by us are conservative estimates. The trend in f_{max} with technology scaling is not clear, the influence of layout, the gate resistance, and other parasitics is very important. The f_{max} data obtained for our NMOS devices are comparable with those from [1], [2], and [8].

Data for NF_{min} were measured for the 250-nm and 180-nm NMOS devices. Data for the minimum noise figure at a frequency of 2 GHz are plotted in Fig. 3 together with data from [1]. NF_{min} decreases strongly with scaling due to an increase in f_t. The high-frequency noise of MOS devices is very low and improves strongly with scaling. Our data is in line with that from [1].

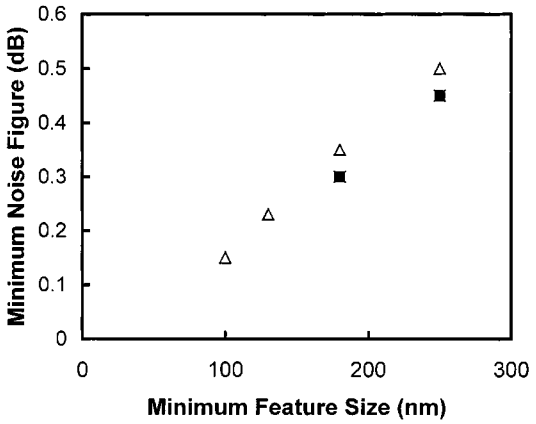

Fig. 3. Data of the minimum noise figure at 2 GHz of NMOS devices versus minimum feature size. (■ Philips data, △ [1]).

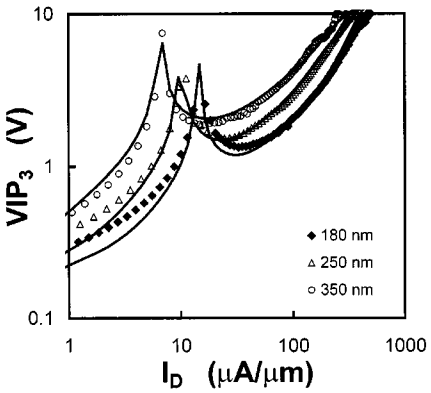

Fig. 4. V_{IP3} data of nominal gate length NMOS devices from 350 nm (○), 250 nm (△), and 180 nm (◆) CMOS technologies. The device width was 10 μm Lines: MOS model 11.

The measured V_{IP3} is plotted in Fig. 4 versus the drain current per micron width. A singularity in V_{IP3} is observed at low current per unit width. This corresponds with a gate bias in the moderate inversion region. The position of the singularity shifts to higher drain current per unit width with scaling toward smaller dimensions. Typical circuit operation is in the moderate inversion region (drain current: 5–50 $\mu\mathrm{A}/\mu\mathrm{m}$). As can be seen in Fig. 4, V_{IP3} changes significantly in this region. For high linearity, V_{IP3} should be large, hence operation in the weak inversion region is not recommended. It appears that for high linearity (i.e., large V_{IP3}) the drain current per unit width has to increase with scaling. Note that the observed V_{IP3} behavior is described well by MOS Model 11 (see Fig. 4). The transition from weak (exponential I–V) to strong inversion (linear I–V) dominates V_{IP3} at low current ($\approx$10 $\mu\mathrm{A}/\mu\mathrm{m}$). At high drain current per micron width (i.e., for high gate drive) velocity saturation and series resistance dominate V_{IP3} [13].

The trend in $1/f$ noise with gate oxide scaling is shown in Fig. 5 for NMOS devices with oxide thickness values between 2 and 20 nm [10]. For low gate bias $S_{v\mathrm{gate}}$ scales roughly with t_{ox}^2, indicating that number fluctuations dominate the $1/f$ noise. At high gate bias $S_{v\mathrm{gate}}$ increases strongly with V_{gt} for thin oxide devices. The gate bias dependence leads to a weaker dependence on oxide thickness. The lines in Fig. 5 are based on the model from Hung *et al.* [12] using the same two parameters for

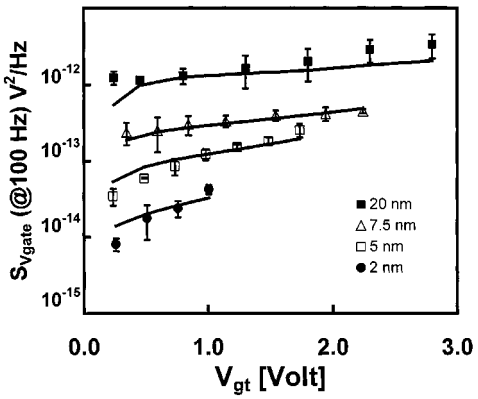

Fig. 5. Input referred spectral noise $S_{v\mathrm{gate}}$ times device area of 10/4 $\mu\mathrm{m}^2$ NMOS devices with variable gate oxide thickness.

all devices. The model of Hung *et al.* describes the technology dependence as well as the dependence on gate and drain bias accurately.

The maximum RF performance of our devices is excellent and in line with that from [1], [2], and [8]. Simulations with the MOS model 11 show good agreement with the experimental RF data for f_{t}, f_{max}, $\mathrm{NF}_{\mathrm{min}}$, NF_{50}, nonlinearity (V_{IP3}), and $1/f$ noise [3], [5]–[7], [10], [13].

V. Simulated RF Performance Trends

The calibrated MOS model 11 has been used to predict the RF performance of the nominal gate length NMOS devices from advanced technologies (down to 50 nm CMOS) from weak inversion conditions ($I_{\mathrm{ds}} \approx 1\ \mu\mathrm{A}/\mu\mathrm{m}$) to strong inversion conditions ($I_{\mathrm{ds}} \approx 1\ \mathrm{mA}/\mu\mathrm{m}$). The supply voltage is scaled from 2.5 V (250 nm) to 0.6 V (50 nm). The RF model contains the MOS device with external gate resistance, junction capacitance, and bulk resistance network. Compact model parameters are estimated using the 1999 ITRS roadmap as a reference. For the gate/drain overlap capacitance, a value of 0.3 $\mathrm{fF}/\mu\mathrm{m}$ was assumed. For a power constrained noise optimization, the device width hardly varies with technology scaling [14]. Practical values of the device width are of the order of several hundreds of micrometers. In the simulations, the device width was fixed at 192 μm. A folded finger layout was used to minimize the gate and bulk resistances and junction capacitance. The finger width was scaled from 3 μm (250 nm CMOS) to 1 μm (50 nm CMOS). The parameters of interest are cutoff frequency (f_{t}), maximum stable gain (g_{msg}), minimum noise figure ($\mathrm{NF}_{\mathrm{min}}$), 50 Ω noise figure (NF_{50}) linearity (V_{IP3}), and the input referred voltage noise spectral density of the $1/f$ noise. Data of g_{msg} are shown instead of f_{max} because g_{msg} is more relevant for actual device operation in the frequency range between 1 and 5 GHz. Note that data are plotted versus the dc drain current per micron width for each technology. This parameter is more relevant for power constrained scaling.

A. Cutoff Frequency

In Fig. 6, the cutoff frequency f_{t} of nominal gate length NMOS devices is plotted as a function of the dc drain current per micron width. A maximum f_{t} higher than 200 GHz is

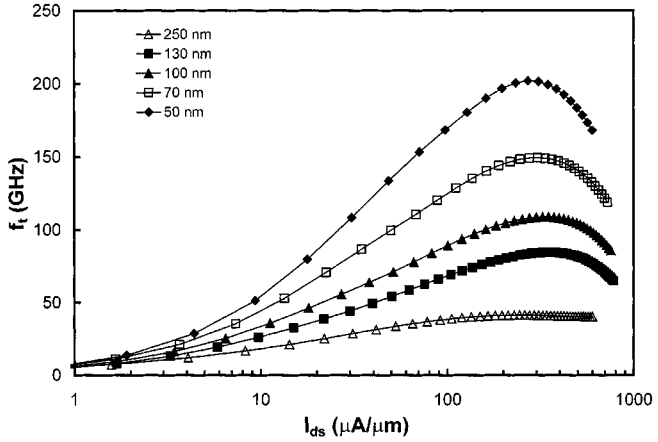

Fig. 6. Simulated cutoff frequency of nominal gate length NMOS devices of 250-nm (△), 130-nm (■), 100-nm (▲), 70-nm (□), and 50-nm (♦) CMOS technologies as function of the drain current per micrometer width. The total device width was 192 μm.

observed for the 50-nm NMOS device. This data is in line with [1]. At low drain current (10 μA/μm) f_t exceeds 50 GHz for 50-nm devices. It appears that both for low (i.e., moderate inversion) and high drain currents (strong inversion) f_t increases with downscaling. The increase per technology is the same $(1.4\times)$ for low and high drain currents. For very low $(\approx 1\ \mu\text{A}/\mu\text{m})$ drain current f_t does not scale. This behavior can be understood from (1).

The gate capacitance per unit width does not scale with technology because of the compensating effects of feature size reduction and increase of oxide capacitance. The transconductance at fixed dc drain current increases with the scaling factor $(1.4\times)$ in moderate and strong inversion. Hence in these regions f_t increases with a factor 1.4 per generation. For weak inversion g_m is proportional to the current (i.e., subthreshold region). Hence for fixed current g_m does not increase. As a result f_t does not scale with technology for weak inversion conditions. For both moderate and strong inversion the cutoff frequency improves significantly. The $1.4\times$ increase in f_t per generation in moderate inversion is very encouraging for future RF CMOS circuits.

B. Maximum Stable Gain

The dependence of g_{msg} on drain current per unit width is shown in Fig. 7 for a frequency of 2 GHz. A maximum g_{msg} of 27 dB is observed. It appears that g_{msg} increases systematically with scaling. g_{msg} is proportional to the transconductance of the device. At fixed current the increase in g_{msg} is approximately 1.5 dB per generation. Very high power gain $(>25\ \text{dB})$ is possible at realistic current for the most advanced technologies.

C. Noise Figure

The minimum noise figure is plotted versus drain current in Fig. 8. The frequency was 2 GHz. $\text{NF}_{\min}$ decreases strongly due to scaling. Our data agree well with [1]. The improvement is significant also at low current. This is mainly due to the increase in f_t. Note that for the noise figure the device width is very important due to impedance matching constraints. For realistic matching networks the device width has to be large (in the order of hundreds of micrometers). To indicate the noise performance at realistic matching conditions NF_{50} data are shown for a 192-μm wide device. In Fig. 9, the noise figure for a real source impedance of 50 Ω (NF_{50} @ 2 GHz) is plotted versus dc drain current per micron width. Note that for this matching condition the device width is even more important. The data are shown as indication only. It appears that NF_{50} decreases strongly with downscaling. It is very encouraging that low NF_{50} $(<1\ \text{dB})$ can be obtained at realistic gate bias conditions.

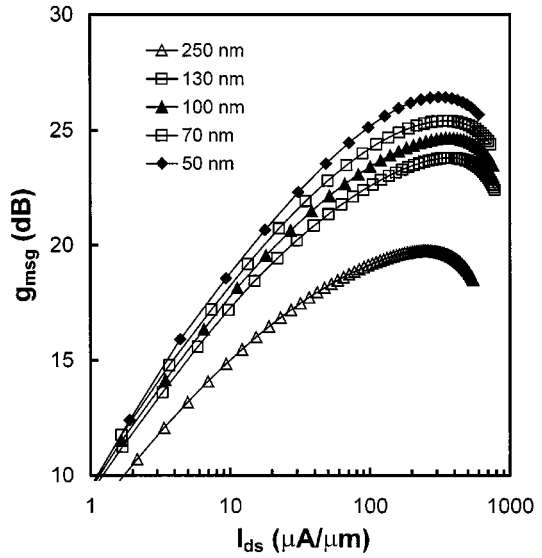

Fig. 7. Simulated maximum stable gain of nominal gate length NMOS devices of 250-nm (△), 130-nm (■), 100-nm (▲), 70 nm (□), and 50-nm (♦) CMOS technologies as function of the drain current per micrometer width. The total device width was 192 μm. The frequency was 2 GHz.

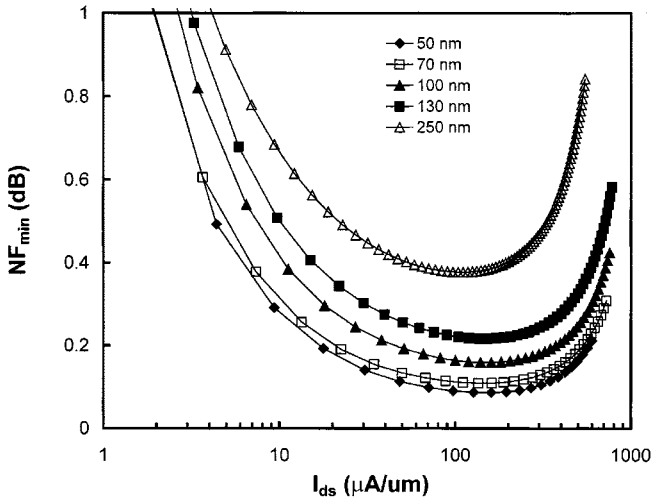

Fig. 8. Simulated minimum noise figure of nominal gate length NMOS devices of 250-nm (△), l30-nm (■), l00-nm (▲), 70-nm (□), and 50-nm (♦) CMOS technologies as function of the drain current per micrometer width. The total device width was 192 μm. The frequency was 2 GHz.

D. Linearity

In Fig. 10, V_{IP3} is plotted for NMOS devices versus drain current per micron width. V_{IP3} depends strongly on drain current (i.e., gate bias). A systematic trend in V_{IP3} is observed. The peak shifts systematically to higher drain current per unit width

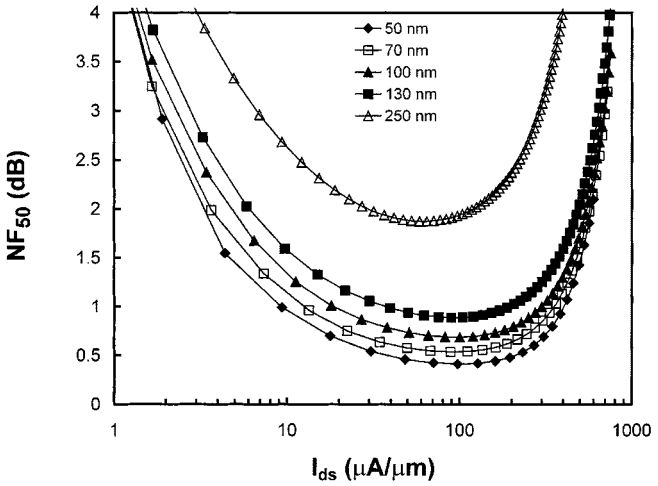

Fig. 9. Simulated 50 Ω noise figures of nominal gate length NMOS devices of 250-nm (△), 130-nm (■), 100-nm (▲), 70-nm (□), and 50-nm (♦) CMOS technologies as function of the drain current per micrometer width. The total device width was 192 μm. The frequency was 2 GHz.

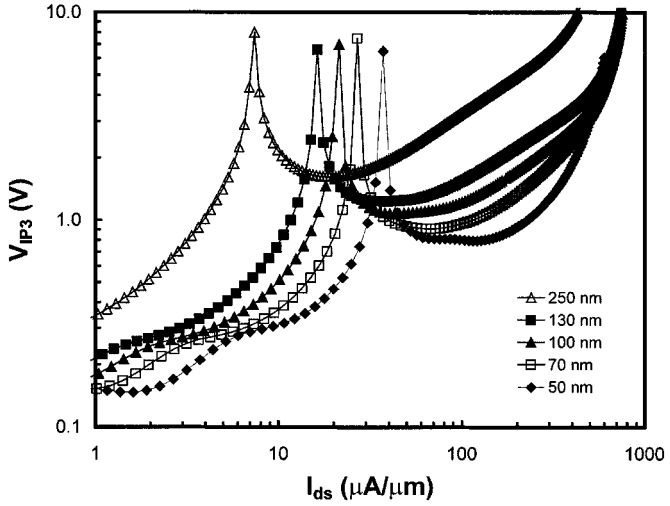

Fig. 10. Simulated third-order voltage intercept point of nominal gate length NMOS devices of 250-nm (△), l30-nm (■), l00-nm (▲), 70-nm (□), and 50-nm (♦) CMOS technologies as function of the drain current per micrometer width. The total device width was 192 μm.

(increase $1.4\times$ per generation). A similar effect was observed in the experimental data in Fig. 4. At high drain current (strong inversion) the linearity parameter degrades slightly with scaling. The shift of the peak toward higher current is not desirable, it implies that a higher current per micron width is needed to preserve linearity. This observation is an important input for the scaling methodology presented in the next section.

E. Low Frequency Noise

Trends in the input referred spectral noise density $S_{v\mathrm{gate}}$ are shown in Fig. 11 for low gate bias ($V_{\mathrm{gt}} = 100$ mV). Experimental data from three CMOS technologies are included. The two noise parameters obtained from the experimental $1/f$ noise data (Fig. 5) were used to predict the trends with scaling. The model data agree well with those obtained from the industrial CMOS technologies. For low gate drive a t_{ox}^2 dependence is predicted. This implies that when the device area is scaled in proportion with the square of the scaling factor the input referred $1/f$ noise spectral density remains the same.

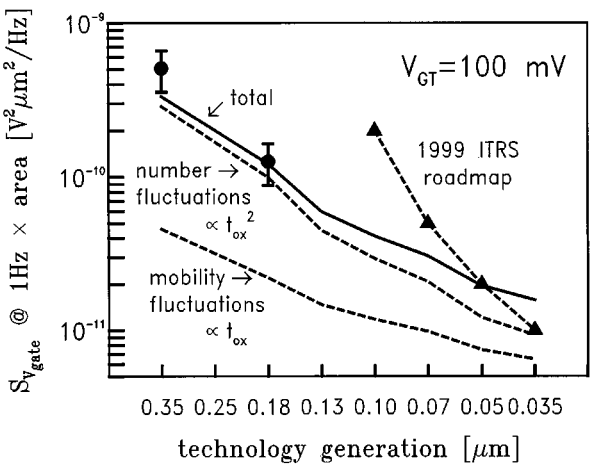

Fig. 11. Solid curve: predicted $S_{v\mathrm{gate}}$ as a function of technology generation for NMOS at $V_{\mathrm{gt}} = 100$ mV. The contributions of the number fluctuation term and the mobility fluctuation term to $S_{v\mathrm{gate}}$ are separately depicted. For comparison the 1999 road map data is added (▲). •: experimental results of existing generations.

TABLE I
SCALING METHODOLOGY

	Scaling factor
Width W	$1/\lambda$
Length L	$1/\lambda$
Supply voltage	$1/\lambda$
Power	$1/\lambda$
Current/width	λ
Total current	1

VI. SCALING METHODOLOGY

The scaling trends presented in the previous section indicate that the RF performance at constant drain current per unit width improves strongly with scaling for the parameters f_{t}, g_{msg},$\mathrm{NF}_{\mathrm{min}}$, and NF_{50}. This holds for both the moderate and strong inversion operating regions. However, the linearity parameter V_{IP3} behaves differently. The drain current per unit width has to increase to maintain a good linearity. Since large signal performance is extremely important for modern RF communication systems a strong degradation in linearity parameters is not desirable. A scaling methodology which limits V_{IP3} degradation is presented below. The methodology is most suited for a transistor in an LNA.

In Table I the scaling trends of the most important parameters are shown. The main assumption in our methodology is that the drain current per unit width must be increased with the scaling factor λ. For a fixed total drain current, this implies that the width has to be scaled down with $1/\lambda$. The supply voltage scales with $1/\lambda$ according to the ITRS roadmap, i.e., from 2.5 V (250 nm) down to 0.6 V (50 nm). Hence the power consumption scales with the same factor $1/\lambda$. The resulting trends in the RF FOM parameters are listed in Table II for an arbitrary total drain current of 5 mA. The major RF parameters f_{t} and $\mathrm{NF}_{\mathrm{min}}$ improve significantly with scaling. The 50 Ω noise figure also improves, a value of 1.1 dB is obtained for the 50-nm technology.

TABLE II
SCALING TRENDS IN RF FOM FOR A TOTAL CURRENT OF 5 mA

Technology	V_{dd} (V)	W (μm)	f_t (GHz)	S_{Vgate} (V^2/Hz) (@ 1Hz)	NF_{min} (dB)	NF_{50} (dB)	g_{msg} (dB)	V_{IP3} (V)
250 nm	2.5	330	19	$4.0\ 10^{-12}$	0.56	1.55	16.8	1.67
130 nm	1.5	150	50	$2.3\ 10^{-12}$	0.30	1.27	20.2	1.24
100 nm	1.2	115	71	$2.4\ 10^{-12}$	0.21	1.19	21.5	1.08
70 nm	0.8	90	112	$2.8\ 10^{-12}$	0.13	1.10	22.8	0.92
50 nm	0.6	65	175	$2.8\ 10^{-12}$	0.10	1.09	24.5	0.81

This is very encouraging, it implies that low-noise figures can be obtained in RF circuits. The $1/f$ noise input referred spectral density remains constant with this scaling methodology. Finally, V_{IP3} degrades slightly for the proposed scaling methodology, nevertheless the decrease is acceptable. From this particular scaling methodology it appears that the RF performance will improve significantly with scaling also at bias conditions relevant for RF applications. Of course other scaling methodologies are possible, for instance when linearity constraints are relaxed significantly better noise performance can be obtained.

VII. SUMMARY

RF performance trends have been studied for NMOS devices from mainline CMOS technologies with feature size down to 50 nm. The RF performance increases strongly with scaling both at high and low drain current (moderate inversion) per unit width. A maximum cutoff frequency above 200 GHz is predicted for the 50-nm NMOS device. The impact of technology scaling on linearity is significant. To maintain a high linearity, the drain current per unit width has to increase for each technology generation. A scaling methodology has been proposed to minimize the linearity degradation while maintaining low power consumption. For this scaling methodology the RF performance metrics improve strongly with down scaling. The results confirm the high potential of CMOS for RF applications at gigahertz frequencies.

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