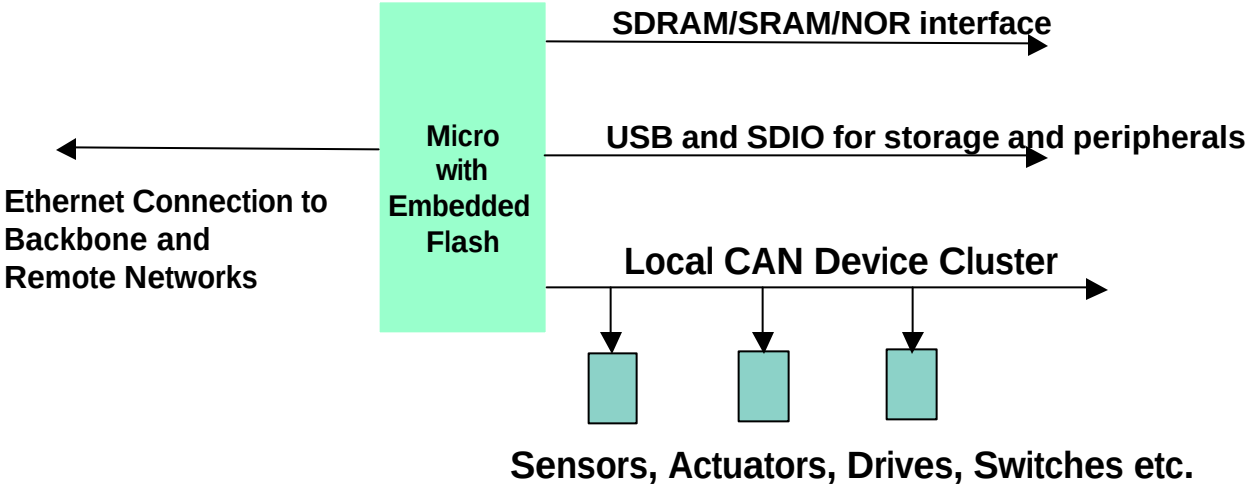
LPC2300 Family
No Bottleneck Ethernet, USB & CAN

Business Line Standard IC's
Product Line Microcontrollers
September 2006

The Challenge

Industrial and Communication Controllers need low-latency processing and full-speed Ethernet processing while maintaining CAN local network and application performance. This requires a 32-bit processor and an efficient bus architecture.



System Architecture Issues

- USB & Ethernet Streams are asynchronous and must both be supported including Isochronous mode USB (1024 byte data bursts)
- Ethernet requires support of 2 concurrent 100Mbits/sec data streams with up to 1500 byte packets
- USB & Ethernet Streams are asynchronous and must both be supported including Isochronous mode USB (1024 byte data bursts)
- CAN, SPI, SSP, SDIO, I^2S, I^2C, UARTs, Timers, PWMs, ADC, DAC, etc, must also be supported but these are all lower bandwidth and packet sizes than Ethernet & USB
- CPU, Ethernet, and USB clock domains (72, 25/50, and 48 MHz) are all separate and need to communicate through memory
- Multi-ported memory is expensive and not desirable

The Goals of the LPC2300 Family

- Manage multiple Asynchronous high-speed channels with no channel performance bottlenecks
- Provide Ethernet, USB, CAN, UART, SPI, and I^2C channels
- Offer a one chip system for high performance and low power at a low cost
- Include industry-leading Embedded Flash operating at SRAM speeds combined with ECC (error correction) for the best performance and power, security and reliability
- Develop a large derivative family in different packages and with different capabilities and memory configurations at different price points, but allowing for easy transitions between family members

Building the LPC2300 – CPU & Memory

- ARM7TDMI-S Processor – 72 MHz
- Up to 512 KB Flash on-chip Flash
  - zero wait-state (execute code from Flash or SRAM)
  - 128-bit wide bus with patented Memory Accelerator Module (MAM)
  - 8-bits Error Correction Code (ECC) for every 128-bit word
  - Automotive qualified Flash process for high reliability
- Up to 58 KB on-chip Static RAM
  - 8 KB – 32 KB SRAM exclusively for CPU
  - 16 KB for Ethernet buffering
  - 8 KB for USB device (code or data)
  - 2 KB for RTC is for data only
  - Additional 4 KB USB FIFO buffer
- Advanced Vectored Interrupt Controller (VIC) – 32 IRQ sources
- Emulation Trace Module supports real-time trace
- Low power - 4 reduced power modes including Deep Power Down

Start with the best embedded Flash in the market

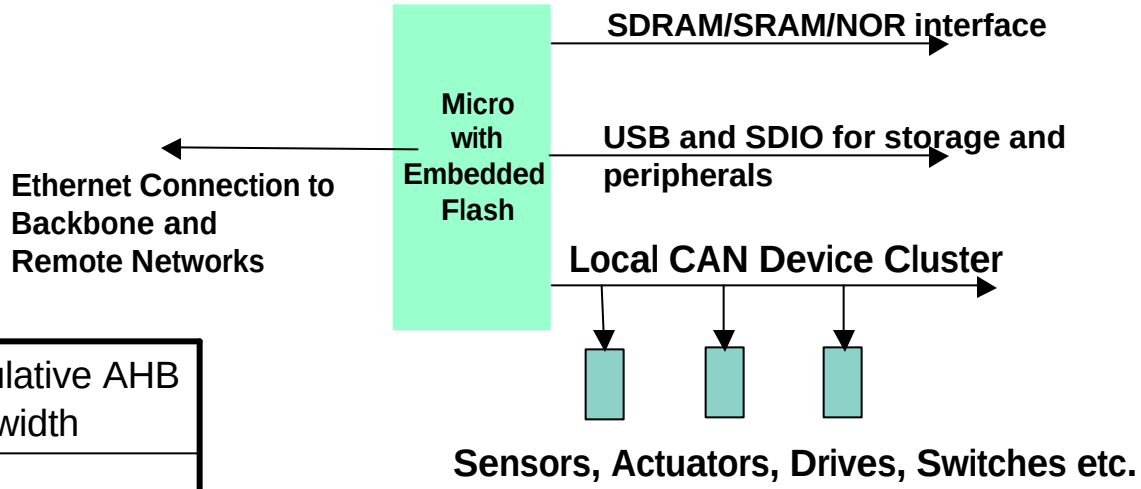
Advantages of On-chip vs. Off-chip Flash

- True Read Security can be implemented
  - Requires real-time encryption/decryption with off-chip Flash
- Greatly reduced power requirement
  - CPU chip and Flash I/O bus do not have to switch every cycle to keep up with ARM CPU (4 bytes every clock cycle)
- Much lower EMI (Electro-Magnetic Interference)
  - Current switching in I/O wires every cycle is eliminated

With a single bus, the CPU, Ethernet and USB all contend for bandwidth, potentially causing a communications “traffic jam”

The solution is the NXP LPC2300 family!

Bus Bandwidth required for Streaming application



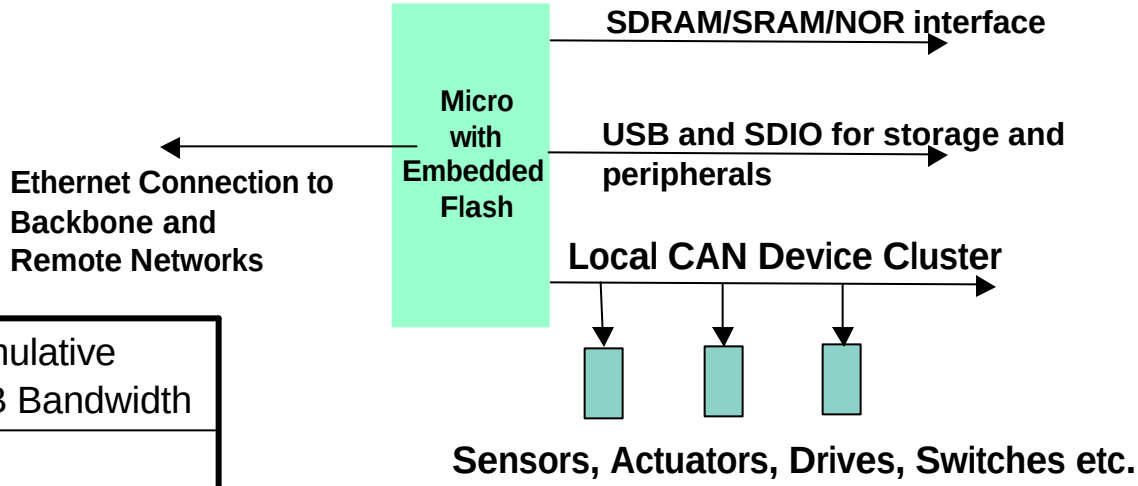
Peripheral	AHB Bus bandwidth %	Cumulative AHB Bandwidth
Ethernet	50	50
USB	4	54
SDI	26	80
I^2S	4	84
$I^2C(2)$	2	86
UARTS(2)	4	90
ADC	8	98

Bus bandwidth usage at 72 MHz

- More than 60% usage of bus bandwidth causes collisions
- Loaded system bandwidth at 72Mhz is 98% for application.

Conclusion:
1 AHB Bus is not sufficient
Multiple Buses and concurrent DMA processing is required

Bus Bandwidth required for Industrial network



Peripheral	AHB Bus bandwidth %	Cumulative AHB Bandwidth
Ethernet	50	50
USB	4	54
Ext, DRAM	20	74
SSP	4	79
I^2C(2)	2	81
CAN (2)	3	84
UARTS(2)	4	88
ADC	8	96

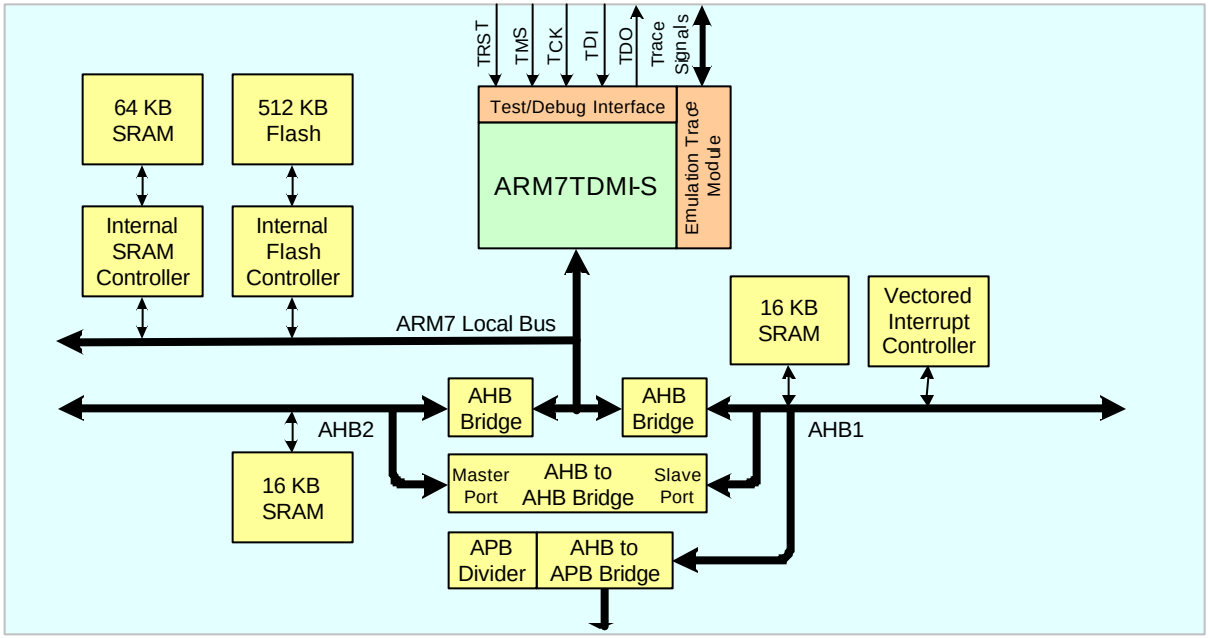
Bus bandwidth usage at 72 MHz

- More than 60% usage of bus bandwidth causes collisions
- Loaded system bandwidth at 72Mhz is 96% for application.

Conclusion:
1 AHB Bus is not sufficient.
Multiple Buses and concurrent DMA processing is required

Building the LPC2300 – Dual AHB Bus

- Two separate but not isolated AHBs
  - Any bus can still reach any other bus through bridges when needed
- High-bandwidth peripherals on different AHBs will not overwhelm the CPU or other peripherals



No communications "traffic jams"!!

The LPC2300 Advantage - parallel buses

- Concurrent operations become possible:
  - Ethernet packet reception and transfer to SRAM
  - CPU Instruction Fetch
  - USB packet reception and transfer to SRAM

- Dedicating AHB Bus to Ethernet is required to guarantee 100 Mbits/sec Ethernet throughput without contention with other peripherals

Building the LPC2300– Ethernet & USB

- Two AHBs allow high performance peripherals to exists without constant arbitration
  - Simultaneous Ethernet DMA, USB DMA and Code execution from Flash
  - Only ARM7 MCU to have no bandwidth constraint
- 3 DMA engines allow concurrent data transfer
- Ethernet MAC with dedicated DMA
  - Direct access to 16KB local RAM
- USB Device with integrated PHY, dedicated DMA and 4KB of RAM
  - Additional 8KB of RAM can be used to buffer heavy USB traffic
- General-Purpose DMA for other peripherals and external memory transfer

The LPC2300 has the only fully-compliant USB available for the ARM7

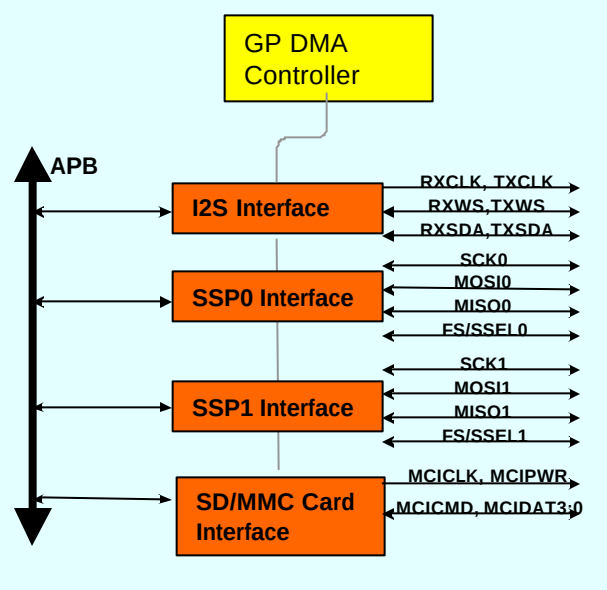
		USB 2.0 Standard	NXP LPC2000	STR7X	ML671xx	SAM7S
Bidirectional Endpoints supported:		16	16	8	3	2
Modes:	Control	Y	Y	Y	Y	Y
	Interrupt	Y	Y	Y	Y	Y
	Bulk	Y	Y	Y	Y	Y
	Isochronous	Y	Y	Y	Y	-
Maximum:	Control Buffer Size	64	64	64	64	64
	Interrupt Buffer Size	64	64	64	64	64
	Bulk Buffer Size	64	64	64	64	64
	Isoch. Buffer Size	1023X2	1023X2	256X2	256X2	None
Frame BW per Transfer		69%	69%	9%	9%	N/A
AHB Bus Access			Yes(DMA)	No (APB)	APB w DMA	No (APB)

LPC2000 USB enables 8.3 Mb/s data throughput

Others can only achieve ~ 1Mb/s

Building the LPC2300 – GP DMA

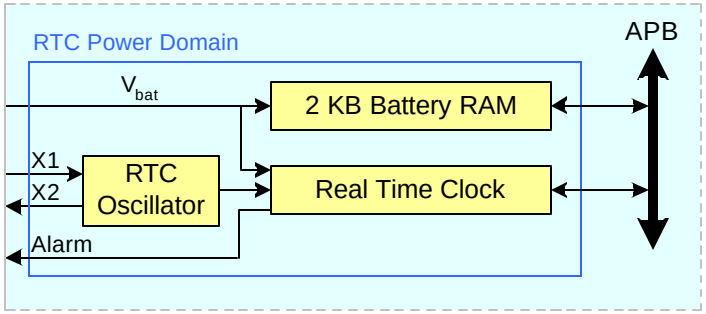
- General Purpose two-channel DMA supports high-speed peripherals as well as memory-to-memory transfers
  - 32-bit AHB master bus width (support 8-, 16-, or 32-bit transfers)
  - Internal four-word FIFO per channel
- Can be used with SD/MMC, two SSP and the I^2S interface
  - Connect peripherals to each other or to memory
- Flexible, customizable DMA performance
  - Big-endian and little-endian support
  - Programmable DMA burst size
  - Hardware DMA channel priority
  - Can generate interrupts



LPC2300 Peripherals

- USB 2.0 Full Speed device with PHY and DMA
  - Supports 32 endpoints and all transfer modes
- CAN 2.0B with two channels
- I^2S interface
- Three I^2C interfaces, SSP, SSP/SPI interfaces
- Four 16C550-type UARTs
- SD/MMC memory card interface
- 8-channel, 10-bit A/D Converter, 10-bit D/A Converter
- 4 MHz on-chip RC-oscillator trimmed to 1% accuracy
- Four 32-bit general purpose timers
- Watchdog timer from multiple clock source options
- PWM block supporting 3 Phase Motor Control
- Low-power Real Time Clock with 2 KB SRAM and battery back-up
- 70 Fast general purpose I/O lines (104 for the LPC2378)
- Single 3.3V power supply (3.0 to 3.6V)

Power Modes



- Power options:
  - On-chip DC-DC converter supplies 1.8V power to all internal logic, except in the RTC power domain.
  - 1.8V power can be supplied from off-chip for some pinouts.

- Power reduction modes:
  - Idle mode: CPU stopped; Peripherals running
  - Sleep mode: All clocks & oscillator off. Flash stays powered for fast wake-up
  - Power Down mode: All clocks & oscillator off. RAM state retained between power cycles
  - Deep Power Down Mode 1: Above + DC-DC off.
  - Deep Power Down Mode 2: All Power OFF except RTC (< 10 uA)

Roadmap

available | In develop.

Functionality

LPC2368 | LPC2378

LPC2366

LPC2364

- Ethernet (RMII)
- USB FS Device
- 2 x CAN

LPC23xx

LPC23xx

LPC24xx

LPC24xx

LPC24xx

- Ethernet (MII+RMII)
- USB FS Device
- USB Host/OTG
- 2 x CAN
- Ext. Memory (SDRAM, SRAM)
- 96K SRAM

Target Applications

Communicate, Process, Monitor

- Industrial control
- Factory automation
- Building automation
- POS systems
- Base stations
- Voice Over IP devices
- Kiosks
- Security systems
- Vending machines
- Protocol conversion
- Computer peripherals
- Medical monitor equipment
- Exercise equipment
- Embedded servers
- Communications module

Ethernet, USB, and CAN Drivers

Ethernet:

- TCP/IP Stacks available from Interniche and Keil (ARM)
- Ethernet Device driver available (NXP web site)

USB:

- USB Device Driver from Keil, Micrium

CAN:

- Development driver ported by Vector

NicheLite for LPC by Interniche

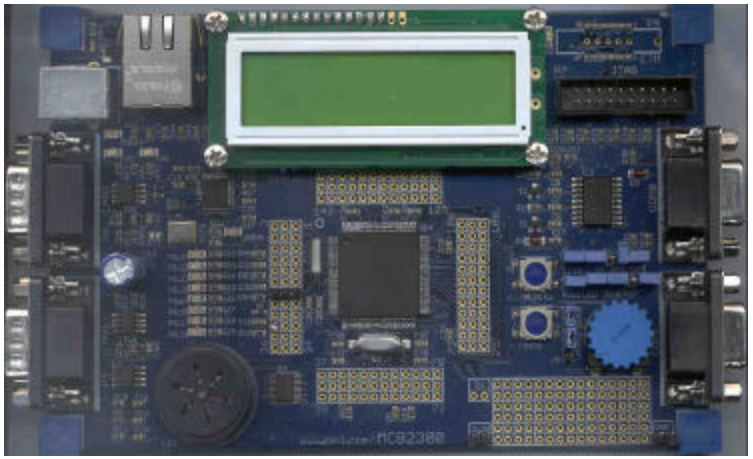
- NicheLite for LPC is a fully featured TCP/IP stack
  - Requires as little as 12 KB of code
- Support for the following protocols:
  - Address Resolution Protocol (ARP), Internet Protocol (IP), Internet Control Message Protocol (ICMP), User Datagram Protocol (UDP), Transmission Control Protocol (TCP), Dynamic Host Configuration Protocol (DHCP) Client, Domain Name System (DNS) Client, Bootstrap Protocol (BOOTP), Trivial File Transfer Protocol (TFTP)
- Includes NicheTask ™ a cooperative multi-tasking scheduler.
- Supports InterNiche's Light Weight API and a Zero-Copy option.
- Single Ethernet interface with device drivers optimized for the LPC2300 and LPC2400
- Example applications (TFTP Client, TFTP Server, HTTP Listener)
- Source code is free to NXP customers
- Support from Interniche at sales@interniche.com
- License - Unlimited use with NXP LPC2000 and LPC3000 microcontrollers only

Development Tools

- Standard ARM JTAG interface compatible with all major ARM tool chains
- Real-Time Emulation Trace Interface
- Real Monitor On-chip Background Debugger for non-invasive Debug (CPU not forced to stop for Debug)
- Development Boards available from Keil (ARM) and Nohau systems
- Free FlashMagic Flash download program supports LPC2300
  - http://www.esacademy.com/software/flashmagic

MCB2300 Evaluation Board from Keil

- Connects to your PC using:
  - Serial port for Flash download using FlashMagic
  - JTAG interface for program debug using the Keil ULINK and µVision IDE and Debugger
- Two board options:
  - MCB2360 with 100 pin LPC2368
  - MCB2370 with 144 pin LPC2378
- Board features:
  - On-chip Ethernet interface
  - USB device interface
  - Two serial interfaces
  - Two CAN interfaces
  - Speaker
  - Analog input (via potentiometer)
  - Eight LEDs



- Available directly from Keil or from NXP's Distributors for $199

Status: Availability, Pricing

- Product is fully bench validated
- Volume production…NOW!
- Samples available
- Pricing starts at $3.99 for 10 Kpcs for LPC2364 (in QFP100)

LPC2300 Series Summary

- No Bottle-Neck Fast Communications Microcontroller
- Ethernet MAC 10/100 full-duplex
  - Reduced Media Independent Interface (RMII)
  - 16KB Buffer + 2nd AHB minimizes CPU interrupt
- USB 2.0 Full Speed Device + on-chip PHY
  - All modes and maximum end-points supported
  - Deep dedicated FIFO (4KB) for maximum performance
- Two CAN 2.0A and 2.0B compliant controllers
- Flexible DMA controller - peripheral and memory-to-memory
- Battery back-up 2KB RAM

Available now!

	Flash	RAM	Ethernet	USB	CAN	DMA	Package
LPC2364	128KB	32KB	RMII	☑	2	☑	QFP100
LPC2366	256KB	56KB	RMII	☑	2	☑	QFP100
LPC2368	512KB	56KB	RMII	☑	2	☑	QFP100
LPC2378	512KB	56KB	RMII	☑	2	☑	QFP144

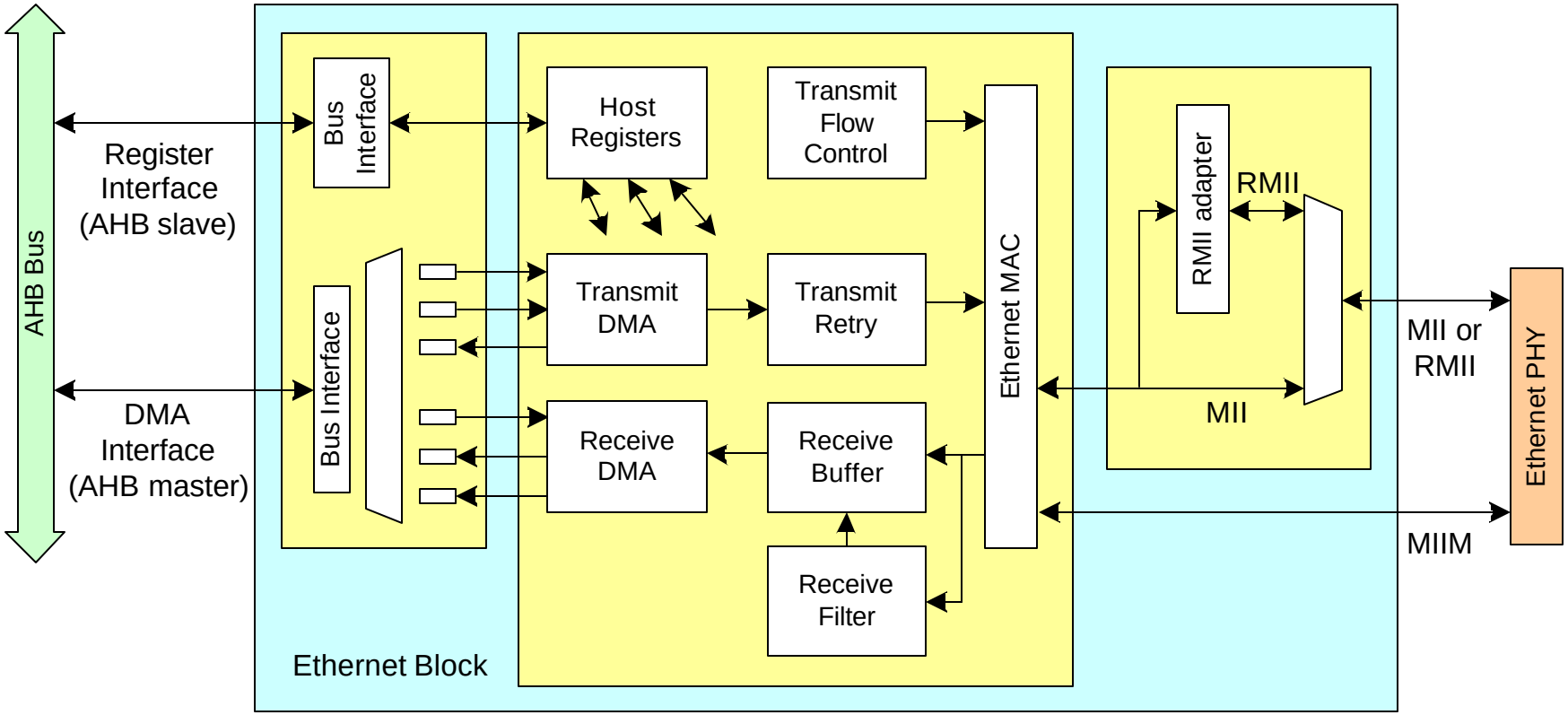
Detailed Technical Slides for Reference

Impact of Ethernet on chip architecture

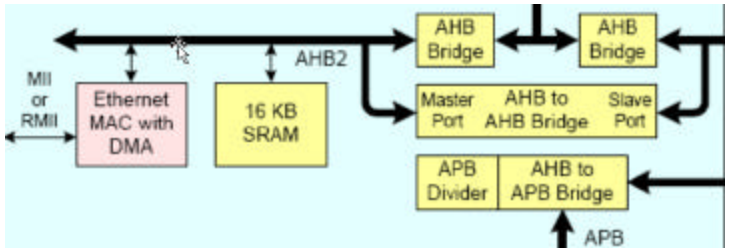
- Full Duplex point-to-point Ethernet (Link segment or Switched) transfers generates up to 200 Mbits/sec Asynchronous packet traffic
  - 100 Mbits in each direction asynchronous data streams
  - 2 separate word transactions every 320 nanoseconds!
  - DMA channel cannot be allowed to wait for long
  - CPU bandwidth can be used up very quickly
- The packets need to be streamed into memory:
  - MAC to receive FIFO via DMA to SRAM to the CPU for processing
  - From the CPU to SRAM to DMA to the transmit FIFO to MAC
  - Not using DMA makes throughput much worse!
- The following overheads need to be considered:
  - Bus contention between the DMA, CPU, and other Bus masters
  - Bus access and status information overhead and DMA descriptor
  - CPU and DMA memory sharing

Detailed technical slides for reference

Ethernet Block Diagram



Embedded Ethernet



Fast Communications Controller

- Independent, but not isolated second AHB bus
- Supports 10/100 Ethernet PHY devices, including:
  - 10 Base-T
  - 100 Base-TX (Level 5 Unshielded Twisted Pair cable)
  - 100 Base-FX (Fiber Optic cable)
  - 100 Base-T4 (Level 3 UTP cable)
- Reduced Media Independent Interface (RMII) bus (2-bit Data RX/TX paths@50 Mhz): 10 Pins
- Fully Compliant with IEEE 802.3X PAUSE MAC Control protocol
  - Full Duplex Flow Control (prevents the loss of outgoing packets during transmission if the switch is sending packets faster than the attached device can receive and process them by sending pause-control frames when its port buffer becomes full)
  - Half Duplex Back Pressure (ensures retransmission of incoming packets if unable to receive incoming packets)

Enhanced Ethernet Features

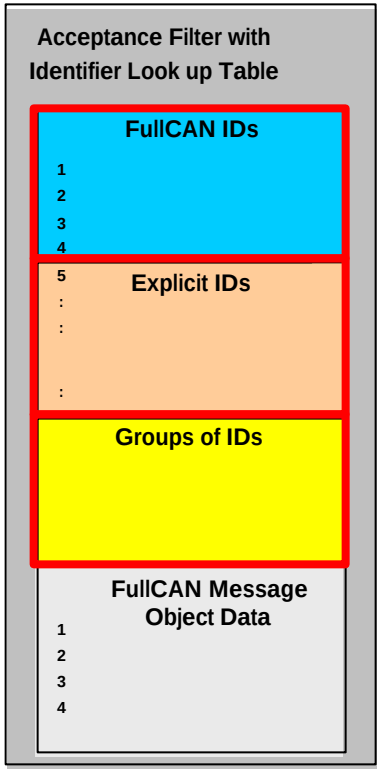
- Receive Filtering
- Multicast and broadcast frame support for both transmit and receive and promiscuous receive mode
- Selectable automatic transmit frame padding and reception with Scatter-Gather DMA off-loads many operations from the CPU
- Over-length frame support for both transmit and receive allows any length frames
- Optional automatic Frame Check Sequence insertion (4-byte CRC) for transmit error correction
- Automatic collision backoff and frame retransmission
- Includes power management by clock switching
- Wake-on-LAN power management support allows system wake-up using the receive filters or a magic packet detection filter

External Ethernet PHY

- LPC2300 interfaces with Ethernet PHYs with RMII interface
- LPC2400 interfaces with Ethernet PHYs with RMII or MII interface
- National Semiconductor's DP83848 PHYTER Family of Ethernet Transceivers have selectable RMII and MII interfaces
  - Other features include Auto-MDIX, 25 MHZ clock output and low power
  - 48 pin LQFP package
  - http://www.ethernet.national.com

CAN Controller Architecture
RAM-based Filtering

- Acceptance controls message reception on all CAN channels
- Acceptance Filter contains:
  - 2 KB Look-up Table RAM for up to **1024 CAN Identifiers**
  - Message Handler
  - Several Identifier sections are programmable
- Programmable Identifier Sections:
  - 11-bit Explicit Identifiers
  - 29-bit Explicit Identifiers
- Groups of 11-bit Identifiers
- Groups of 29-bit Identifiers
- FullCAN compatibility mode



CAN Block Benchmark Test

Benchmark Test Setup:

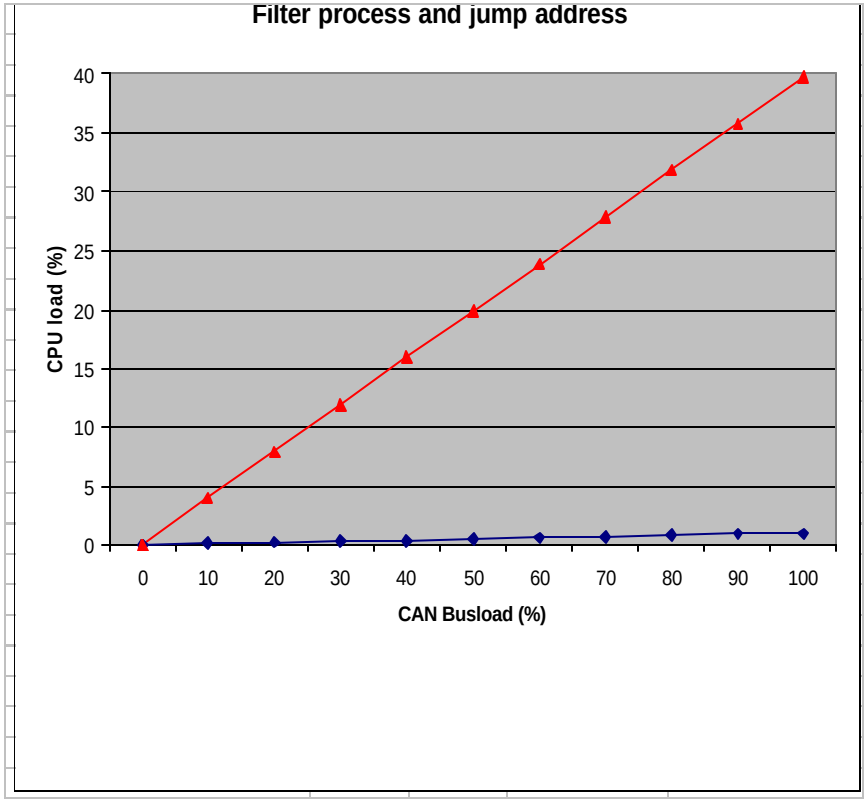
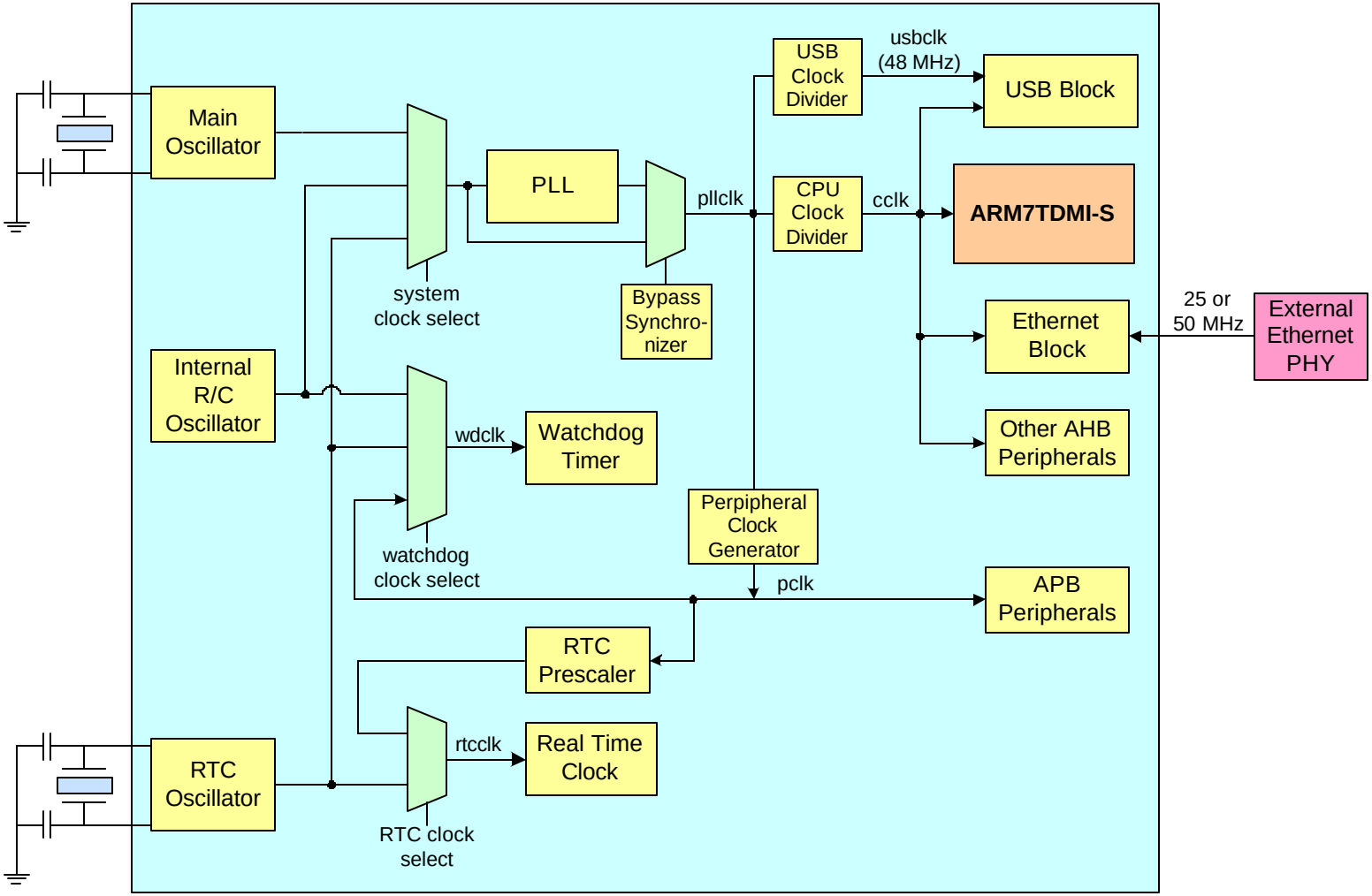
- Dhrystone 2.1 test runs as background load for the ARM7 CPU
- Dhrystone is interrupted by:
  - Timer Interrupt (every 1 ms)
  - CAN Receive Interrupts -> Action Handler
  - CAN Transmit Interrupts
- CAN bit-rate is 500kbit/s on all (6) channels
- LPC microcontroller performs CAN message routing on 6 channels
  - Received messages are routed from channel ***n*** to ***n+1 (wrap-around)***
  - CAN Identifier is changed, data bytes are mirrored in routed messages
- Benchmark test is performed for CAN bus-loads 0….90%
- Software is executed from internal flash @ 60MHz

Hardware Acceptance Filter

CPU load required for filtering incoming messages and jumping to the interrupt service routine

Assumptions

- 6 CAN buses @ 500 kbit/s
- 80% of all incoming messages are accepted
- 50% Standard Frame Format (SFF) and 50% Extended Frame Format (EFF)
- Each message contains 4 data bytes on average
- CPU running @ 60 MHz



Building the LPC2300 – Clock Source