

# A5G21H605W19N

Airfast RF Power GaN Amplifier

Rev. 4.0 — 12 February 2026

Product data sheet



## 1 General description

This 85 W asymmetrical Doherty RF power GaN amplifier is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2110 MHz to 2200 MHz.

This part is characterized and performance is guaranteed for applications operating in the 2110 MHz to 2200 MHz band. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

## 2 Features and benefits

- High terminal impedances for optimal broadband performance
- Advanced high performance in-package Doherty
- Improved linearized error vector magnitude with next generation signal
- Able to withstand extremely high output VSWR and broadband operating conditions
- Plastic package

## 3 Typical performance

**Table 1. 2100 MHz — Typical Doherty single-carrier W-CDMA reference circuit performance**

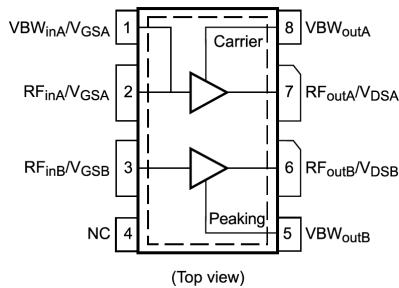
$V_{DD} = 48 \text{ Vdc}$ ,  $I_{DQA} = 300 \text{ mA}$ ,  $V_{GSB} = -5.0 \text{ Vdc}$ ,  $P_{out} = 85 \text{ W Avg.}$ , Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.<sup>[1]</sup>

Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)
2110 MHz	16.3	56.1	8.9	-26.3
2140 MHz	16.5	57.6	8.6	-27.3
2170 MHz	16.2	57.1	8.2	-28.9

[1] All data measured with device soldered to NXP reference circuit.



## 4 Pinning information



**Note:** Exposed backside of the package is the source terminal for the amplifier.

Figure 1. Pin configuration

## 5 Ordering information

Table 2. Ordering information

Device	Tape and Reel Information	Package
A5G21H605W19NR3	R3 Suffix = 250 Units, 44 mm Tape Width, 13-inch Reel	OM-780-4S4S

## 6 Product marking

A5G21H605W19N  
AAWLYYWWZZ

Figure 2. Product marking

Table 3. Product marking trace code

Identifier	Description
AA	Assembly location
WL	Wafer lot indicator
YYWW	Date code
ZZ	Assembly lot

## 7 Limiting values

Table 4. Limiting values

Rating	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	125	Vdc
Gate-Source Voltage	V <sub>GS</sub>	-16, 0	Vdc
Operating Voltage	V <sub>DD</sub>	55	Vdc
Maximum Forward Gate Current, I <sub>G (A+B)</sub> , @ T <sub>C</sub> = 25°C	I <sub>GMAX</sub>	90	mA
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Case Operating Temperature Range	T <sub>C</sub>	-55 to +150	°C
Maximum Channel Temperature	T <sub>CH</sub>	225	°C

## 8 Recommended operating conditions

Table 5. Recommended operating conditions

Characteristic	Symbol	Value	Unit
Operating Voltage	V <sub>DD</sub>	48	Vdc

## 9 Thermal characteristics

Table 6. Thermal characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance by Infrared Measurement, Active Die Surface-to-Case Case Temperature 124°C, P <sub>D</sub> = 95 W	R <sub>θSC</sub> (IR)	0.46 <sup>[1]</sup>	°C/W
Thermal Resistance by Finite Element Analysis, Channel-to-Case Case Temperature 124°C, P <sub>D</sub> = 94.8 W	R <sub>θCHC</sub> (FEA)	0.8 <sup>[2]</sup>	°C/W

[1] Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <https://www.nxp.com/RF> and search for AN1955.

[2] R<sub>θCHC</sub> (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = 10<sup>[A + B/(T + 273)]</sup>, where T is the channel temperature in degrees Celsius, A = -11.6 and B = 9129.

## 10 ESD protection characteristics

Table 7. ESD protection characteristics

Test Methodology	Class
Human Body Model (per JS-001-2017)	2
Charge Device Model (per JS-002-2014)	C3

## 11 Moisture sensitivity level

Table 8. Moisture sensitivity level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	245	°C

## 12 Electrical characteristics

### 12.1 DC characteristics — off characteristics

Table 9. DC characteristics — off characteristics

 $(T_A = 25^\circ\text{C} \text{ unless otherwise noted})$ 

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Off characteristics<sup>[1]</sup></b>					
Off-State Drain Leakage ( $V_{DS} = 150 \text{ Vdc}$ , $V_{GS} = -8 \text{ Vdc}$ ) Carrier ( $V_{DS} = 150 \text{ Vdc}$ , $V_{GS} = -8 \text{ Vdc}$ ) Peaking	$I_{D(BR)}$	—	—	13.2 26.4	mAdc

[1] Each side of device measured separately.

### 12.2 DC characteristics — on characteristics

Table 10. DC characteristics — on characteristics

 $(T_A = 25^\circ\text{C} \text{ unless otherwise noted})$ 

Characteristic	Symbol	Min	Typ	Max	Unit
<b>On characteristics — Side A, Carrier</b>					
Gate Threshold Voltage ( $V_{DS} = 10 \text{ Vdc}$ , $I_D = 30 \text{ mAdc}$ )	$V_{GS(th)}$	-4.6	-2.6	-1.9	Vdc
Gate Quiescent Voltage ( $V_{DD} = 48 \text{ Vdc}$ , $I_{DA} = 300 \text{ mAdc}$ , Measured in Functional Test)	$V_{GSA(Q)}$	-3.1	-2.6	-2.1	Vdc
<b>On characteristics — Side B, Peaking</b>					
Gate Threshold Voltage ( $V_{DS} = 10 \text{ Vdc}$ , $I_D = 60 \text{ mAdc}$ )	$V_{GS(th)}$	-4.6	-2.6	-1.9	Vdc

### 12.3 Functional tests

Table 11. Functional tests

(In NXP Doherty Production Test Fixture,  $T_A = 25^\circ\text{C}$  unless otherwise noted, 50 ohm system)<sup>[1]</sup>  $V_{DD} = 48 \text{ Vdc}$ ,  $I_{DQA} = 300 \text{ mA}$ ,  $V_{GSB} = (V_t - 1.87) \text{ Vdc}$ ,  $P_{out} = 85 \text{ W Avg.}$ ,  $f = 2140 \text{ MHz}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5 \text{ MHz}$  Offset.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	$G_{ps}$	13.7	15.1	18.0	dB
Drain Efficiency	$\eta_D$	48.0	55.3	—	%
Saturated Power (Pulsed CW, 5% Duty Cycle)	$P_{sat}$	56.6	57.9	—	dBm
Adjacent Channel Power Ratio	ACPR	—	-29.6	-22.0	dBc

[1] Internally matched part.

## 12.4 Wideband ruggedness

**Table 12. Wideband ruggedness**

(In NXP Doherty Production Test Fixture,  $T_A = 25^\circ\text{C}$  unless otherwise noted, 50 ohm system)  $I_{DQA} = 300 \text{ mA}$ ,  $V_{GSB} = -4.5 \text{ Vdc}$ ,  $f = 2140 \text{ MHz}$ , Additive White Gaussian Noise (AWGN) with 10 dB PAR.

Characteristic	Symbol	Min	Typ	Max	Unit
ISBW of 400 MHz at 55 Vdc, 123 W Avg. Modulated Output Power (3 dB Input Overdrive from 85 W Avg. Modulated Output Power)			No Device Degradation		

## 12.5 Typical performance

**Table 13. Typical performance**

(In NXP Doherty Fixture,  $T_A = 25^\circ\text{C}$  unless otherwise noted, 50 ohm system)  $V_{DD} = 48 \text{ Vdc}$ ,  $I_{DQA} = 300 \text{ mA}$ ,  $V_{GSB} = -4.8 \text{ Vdc}$ , 2110–2170 MHz Bandwidth.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Pulsed CW, 10% duty cycle</b>					
Saturated Power <sup>[1]</sup>	$P_{\text{sat}}$	—	676	—	W
AM/PM <sup>[1]</sup> (Maximum value measured at saturated power across the 2110–2170 MHz bandwidth)	$\Phi$	—	-25	—	°
Gain Variation @ Avg. Power over Temperature <sup>[2]</sup> (-40°C to +85°C)	$\Delta G$	—	0.016	—	dB/°C
Output Power Variation @ Saturated Power over Temperature <sup>[2]</sup> (-40°C to +85°C)	$\Delta P_{\text{sat}}$	—	0.0035	—	dB/°C
<b>Single-carrier W-CDMA unclipped</b>					
Gain Flatness in 60 MHz Bandwidth @ $P_{\text{out}} = 85 \text{ W Avg.}$ <sup>[1]</sup>	$G_F$	—	1.5	—	dB
<b>2-tone CW</b>					
VBW Resonance Point <sup>[1]</sup> (IMD Third Order Intermodulation Inflection Point)	$\text{VBW}_{\text{res}}$	—	240	—	MHz

[1] All data measured with device soldered to NXP characterization fixture.

[2] All data measured in NXP production fixture.

## Correct biasing sequence for GaN depletion mode amplifiers in a Doherty configuration

### Bias ON the device

1. Set gate voltage  $V_{GSA}$  and  $V_{GSB}$  to -5 V.
2. Set drain voltage  $V_{DSA}$  and  $V_{DSB}$  to nominal supply voltage (+48 V).
3. Increase  $V_{GSA}$  (carrier side) until  $I_{DQA}$  current is attained.
4. Increase  $V_{GSB}$  (peaking side) to target bias voltage.
5. Apply RF input power to desired level.

### Bias OFF the device

1. Disable RF input power.
2. Adjust gate voltage  $V_{GSA}$  and  $V_{GSB}$  to -5 V.
3. Adjust drain voltage  $V_{DSA}$  and  $V_{DSB}$  to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.

4. Disable  $V_{GSA}$  and  $V_{GSB}$ .

## 13 Component layout and parts list

### 13.1 Component layout

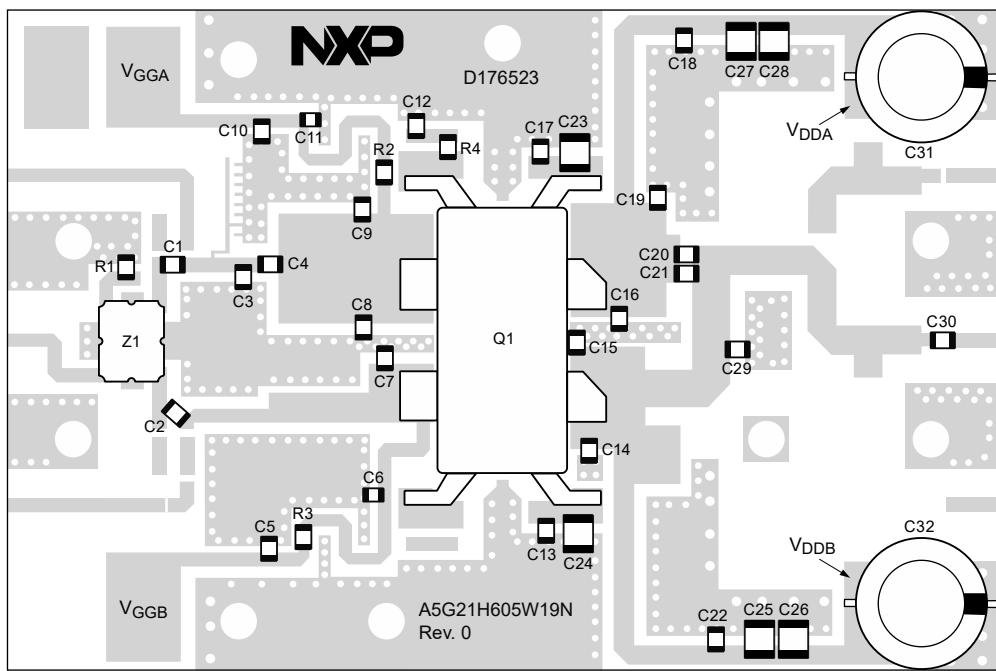


Figure 3. A5G21H605W19N reference circuit component layout — 2.0" (5.1 cm) x 3.0" (7.6 cm)

### 13.2 Component designations and values

Table 14. A5G21H605W19N reference circuit component designations and values

Part	Description	Part Number	Manufacturer
C1, C2, C4, C13, C17, C18, C22	12 pF Chip Capacitor	GQM2195C2E120FB12D	Murata
C3	0.8 pF Chip Capacitor	600F0R8BT250XT	ATC
C5, C10, C12	1.0 $\mu$ F Chip Capacitor	GJ821BR71H105KA12L	Murata
C6, C11	12 pF Chip Capacitor	GQM1875C2E120FB12D	Murata
C7	0.75 pF Chip Capacitor	GQM2195C2ER75BB12D	Murata
C8	1.0 pF Chip Capacitor	600F1R0BT250XT	ATC
C9, C19	0.5 pF Chip Capacitor	GQM2195C2ER50BB12D	Murata
C14	0.8 pF Chip Capacitor	GQM2195C2ER80BB12D	Murata
C15	1.8 pF Chip Capacitor	600F1R8BT250XT	ATC
C16	0.2 pF Chip Capacitor	600F0R2BT250XT	ATC
C20	1.1 pF Chip Capacitor	600F1R1BT250XT	ATC
C21	1.2 pF Chip Capacitor	600F1R2BT250XT	ATC
C23, C24, C25, C26, C27, C28	10 $\mu$ F Chip Capacitor	C3225X7S1H106K	TDK
C29	0.3 pF Chip Capacitor	600F0R3BT250XT	ATC
C30	12 pF Chip Capacitor	600F120JT250XT	ATC
C31, C32	470 $\mu$ F, 100 V Electrolytic Capacitor	MCGPR100V477M16X32	Multicomp
Q1	RF Power GaN Amplifier	A5G21H605W19N	NXP
R1	50 $\Omega$ , 8 W Termination Chip Resistor	C8A50Z4B	Anaren
R2, R3	3.3 $\Omega$ , 1/8 W Chip Resistor	CRCW08053R30NEA	Vishay
R4	10 $\Omega$ , 1/8 W Chip Resistor	RK73H2ATTS10R0F	KOA Speer
Z1	1800–2300 MHz, 90°, 3 dB Hybrid Coupler	X3C21P1-03S	Anaren
PCB	Rogers RO4350B, 0.020", $\epsilon_r$ = 3.66	D176523	MTL

## 14 Package information

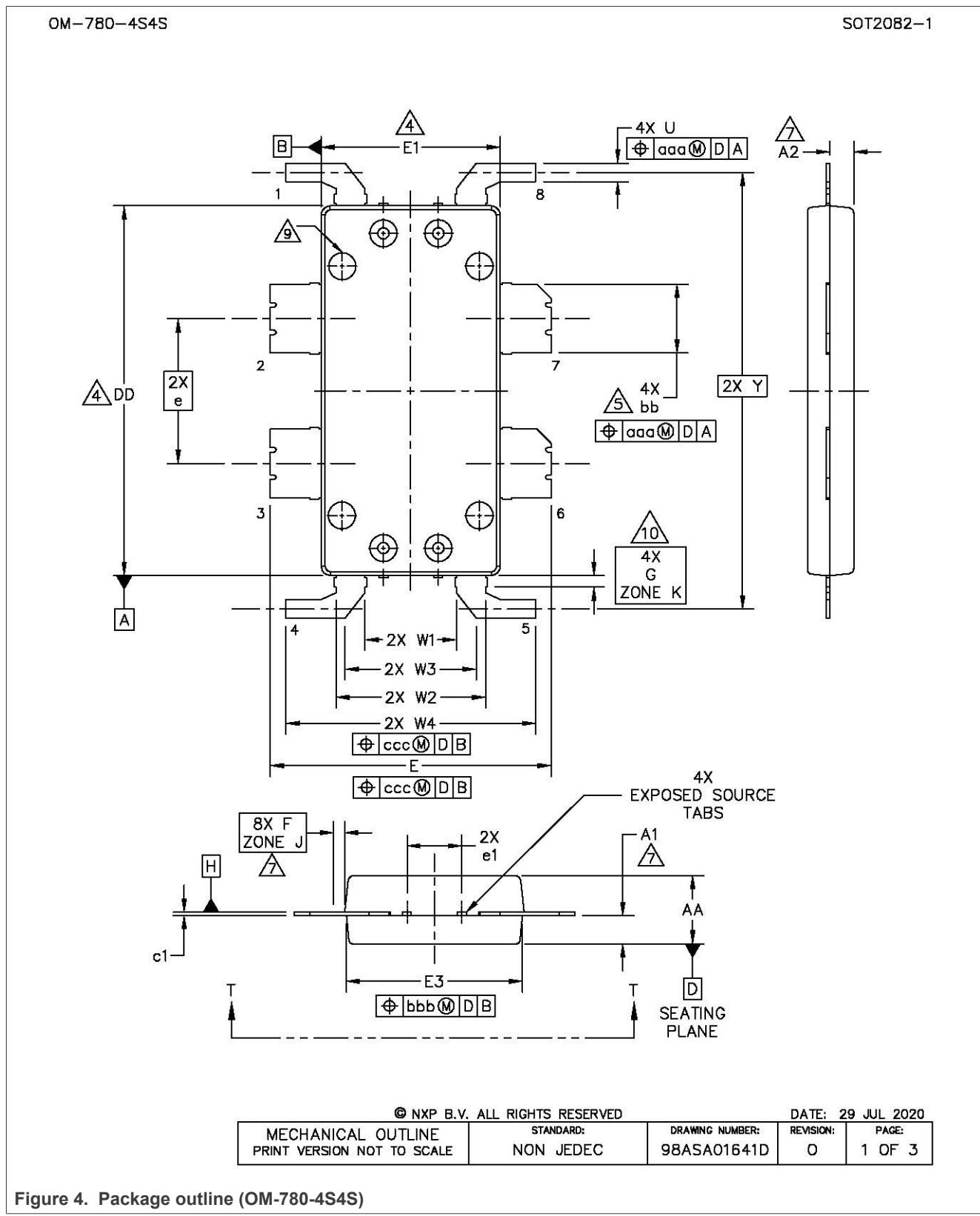
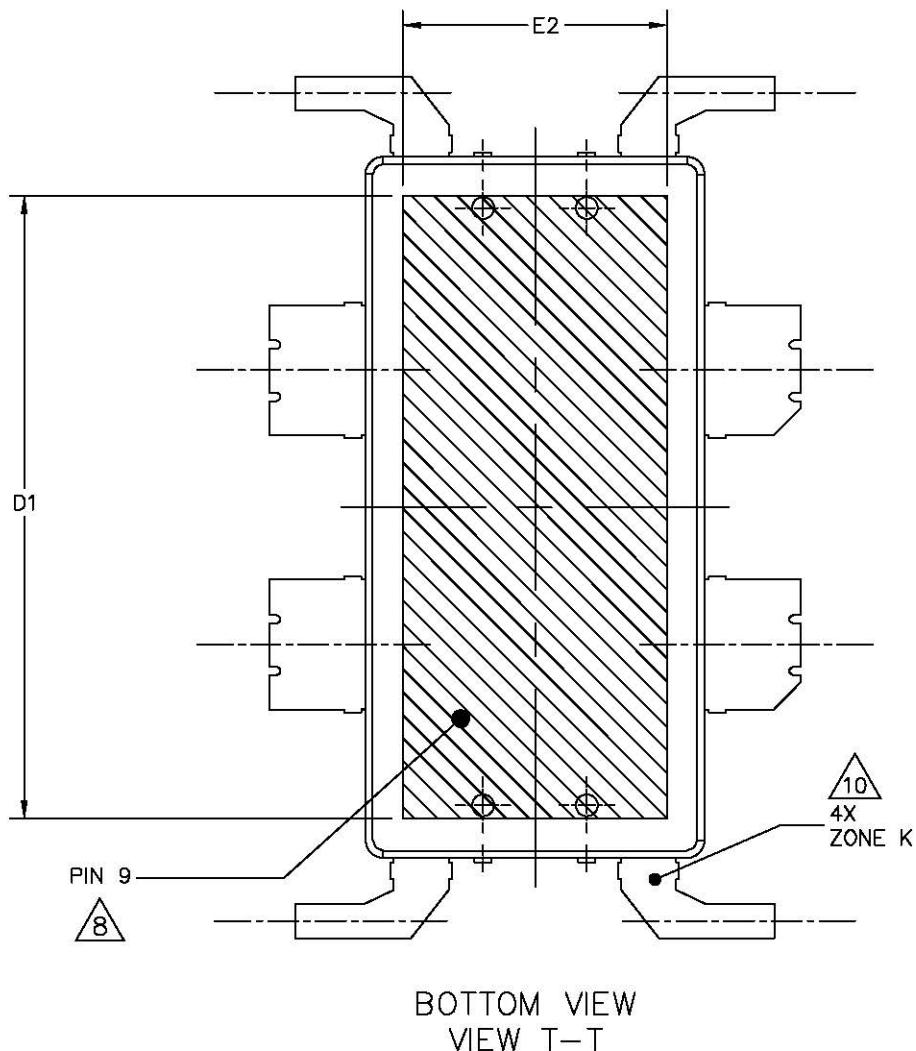


Figure 4. Package outline (OM-780-4S4S)

OM-780-4S4S

SOT2082-1



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Figure 5. Package outline (OM-780-4S4S) — bottom view

OM-780-4S4S

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## NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSIONS A1 AND A2 APPLIES WITHIN ZONE J ONLY. A1 APPLIES TO PINS 2, 3, 6 AND 7. A2 APPLIES TO PINS 1, 4, 5 AND 8.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.
9. DIMPLED HOLE REPRESENTS INPUT SIDE.
10. ZONE K REPRESENTS NON-SOLDERABLE REGION WHERE MOLD FLASH AND RESIN BLEED ARE PERMITTED ON BOTH SIDES OF THE LEADS.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	.148	.152	3.76	3.86	W2	.321	.331	8.15	8.41
A1	.059	.065	1.50	1.65	W3	.281	.291	7.14	7.39
A2	.056	.068	1.42	1.73	W4	.538	.554	13.67	14.07
DD	.808	.812	20.52	20.62	U	.037	.043	0.94	1.09
D1	.720	----	18.29	----	Y	.956 BSC		24.28 BSC	
E	.610	.618	15.49	15.70	bb	.147	.153	3.73	3.89
E1	.390	.394	9.91	10.01	c1	.007	.011	0.18	0.28
E2	.306	----	7.77	----	e	.317 BSC		8.05 BSC	
E3	.383	.387	9.73	9.83	e1	.116	.124	2.95	3.15
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
G	.030 BSC		0.76 BSC		bbb	.006		0.15	
W1	.195	.205	4.95	5.21	ccc	.010		0.25	

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Figure 6. Package outline (OM-780-4S4S) — notes, dimensions

## 15 Product documentation, software and tools

Refer to the following resources to aid your design process.

### Application notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Software

- .s2p File

### Development tools

- Printed Circuit Boards

## 16 Revision history

The following table summarizes revisions to this document.

Table 15. Revision history

Document ID	Release date	Description
A5G21H605W19N v.4.0	12 February 2026	<ul style="list-style-type: none"><li>• Fixed <a href="#">Figure 1</a></li></ul>
A5G21H605W19N v.3.0	28 January 2026	<ul style="list-style-type: none"><li>• Changed reference of "Transistor" to "Amplifier"</li></ul>
A5G21H605W19N v.2	2 May 2025	<ul style="list-style-type: none"><li>• Fig. 2, Product marking: updated, p. 2</li><li>• Table 3, Product marking trace code: updated, p. 2</li></ul>
A5G21H605W19N v.1	21 December 2023	<ul style="list-style-type: none"><li>• Table 8, Moisture Sensitivity Level: package peak temperature updated to reflect actual test data, p. 3</li></ul>
A5G21H605W19N v.0	14 August 2023	<ul style="list-style-type: none"><li>• Initial release of data sheet</li></ul>

## Legal information

### Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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