P3T1750DP

I3C, I2C-Bus Interface, 1 °C Accuracy, Digital Temperature Sensor

Rev. 1.2 — 8 October 2025 **Product data sheet**

Document information

Information	Content
Keywords	P3T1750DP, data sheet, I2C-bus, I3C, digital temperature sensor
Abstract	P3T1750DP is a temperature-to-digital converter from -40 °C to +125 °C range.

1 General description

The P3T1750DP is a temperature-to-digital converter from -40 °C to +125 °C range. It uses an on-chip band gap temperature sensor and A-to-D conversion technique with an overtemperature detection. The device contains various configuration and data registers to store the device settings, such as device operation mode, and a temperature register (Temp) to store the digital temp reading that a controller can communicate via the 2-wire serial I3C (up to 12.5 MHz) and I2C (up to 3.4 MHz) interface.

The I2C interface supports up to 32 target addresses and an alert function, which becomes active when the temperature exceeds the programmed limits.

The I3C interface supports IBI (In Band Interrupt) where P3T1750DP emits its address into the arbitrated address header on the I3C bus. This operation is done to notify the controller of an interrupt. It does not require an additional interrupt pin.

The P3T1750DP can be configured for different operation conditions. It can be set in normal mode to monitor the ambient temperature periodically, or in shut-down mode to minimize power consumption. The temperature register always stores a 12-bit two's complement data, giving a temperature resolution of 0.0625 °C.

The Alert output operates in either of two selectable modes: Alert comparator mode or Alert interrupt mode. Its active state can be selected as either HIGH or LOW. The fault queue that defines the number of consecutive faults to activate the Alert output is programmable and the set-point limits.

2 Features and benefits

- I3C (up to 12.5 MHz) and I2C (up to 3.4 MHz) interface
  - 32 I2C target addresses
  - 32 I3C Provisional-ID
- Supply range: 1.4 V to 3.6 V
- Programmable overtemperature alerts
- Resolution: 12 bits (0.0625 °C)
- Accuracy:
  - 1.4 V < V_{CC} < 3.6 V
    - ±1 °C (maximum) from -40 °C to +125 °C
- Low quiescent current: 4.1 µA supply current (typical)
- ESD protection exceeds 2000 V HBM per JS-001-2017 and 1000 V CDM per JS-002-2018
- Package: TSSOP8
- P3T1750DP /Q900 for automotive

3 Applications

- IoT
- Portable devices
- SSD
- Industrial controllers
- Servers
- PC/Notebook
- Automotive (P3T1750DP /Q900)

4 Ordering information

Table 1 describes the ordering information for P3T1750DP.

Table 1. Ordering Information

Type number	Topside mark	Package		
		Name	Description	Version
P3T1750DP	P1750	TSSOP8	Plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
P3T1750DP /Q900[1]	Q1750	TSSOP8	Plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

[1] P3T1750DP /Q900 is AEC-Q100 compliant. Contact NXP sales for PPAP.

4.1 Ordering options

Table 2 describes the ordering options for P3T1750DP.

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
P3T1750DP	P3T1750DP Z	TSSOP8	Reel 13” Q1/T1 *standard mark SMD SSB[1]	2500	T_{amb} = -40 °C to +125 °C
P3T1750DP /Q900	P3T1750DP /Q900Z	TSSOP8	Reel 13” Q1/T1 *standard mark SMD SSB [1]	2500	T_{amb} = -40 °C to +125 °C

[1] This packing method uses a Static Shielding Bag (SSB) solution. Material must be kept in a sealed bag between uses.

5 Block diagram

Figure 1 shows the labeled block diagram of P3T1750DP.

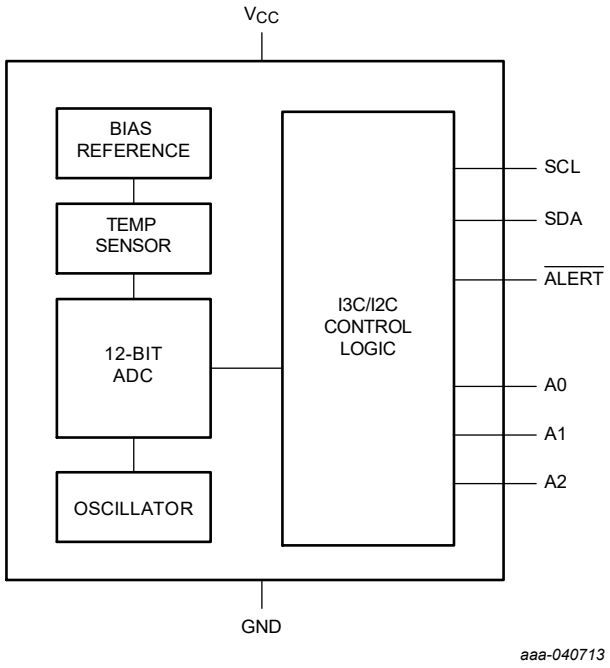


Figure 1. Block diagram

6 Pinning information

This section provides the pin configuration and description of the TSSOP8 package.

6.1 Pinning

Figure 2 shows the pin configuration for TSSOP8 package.

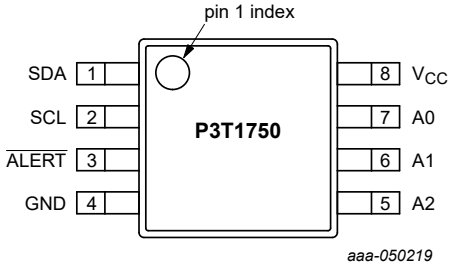


Figure 2. TSSOP8 pin configuration

6.2 Pinning description

Table 3 provides detailed description of the various pins on TSSOP8 package.

Table 3. TSSOP8 pin description

Symbol	Pin	Description
SDA	1	Digital I/O. I3C/I2C-bus serial bidirectional data line.
SCL	2	Digital input. I3C/I2C-bus serial clock.
ALERT	3	Alert open-drain output.

Table 3. TSSOP8 pin description*...continued*

Symbol	Pin	Description
GND	4	Ground.
A2	5	Digital input. User-defined address bit 2.
A1	6	Digital input. User-defined address bit 1.
A0	7	Digital input. User-defined address bit 0.
V_{CC}	8	Power supply.

7 Functional description

7.1 General operation

The P3T1750DP uses the on-chip band gap sensor to measure the device temperature with the resolution of 0.0625 °C and stores the 12-bit two's complement digital data, resulted from 12-bit A-to-D conversion, into the device Temp register. A controller on the I3C/I2C-bus can read this Temp register anytime. Reading temperature data does not affect the conversion in progress during the read operation. The temperature range is from -40 °C to 125 °C.

The P3T1750DP can be set to operate in three modes: one-shot, continuous conversion or shutdown mode through OS, TM and SD bits in the configuration register, allowing the user flexibility for different mode operations.

7.2 I2C-bus serial interface

The device can be connected to a compatible 2-wire serial interface Fast-mode Plus I2C-bus as a target device under the control of a controller or controller device, using two device terminals: SCL and SDA. The controller must provide the SCL clock signal and write/read data to/from the device through the SDA terminal. If the I2C-bus common pullup resistors are not installed as required for I2C-bus, then an external pullup resistor, about 5 kΩ, is needed for each of these two terminals. Section 7.6 describes the bus communication protocols.

7.3 Target and mode description

7.3.1 Target address

To communicate with the device, the controller must first address target devices via a target address byte. The target address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation. The device features three address pins to allow up to 32 devices to be addressed on a single bus interface (for details, see Table 4).

P3T1750DP requires 20 ms (max) after $V_{CC} \geq V_{POR}$ (1.2 V(max)) to recognize I2C/I3C command. After that, pin A0/A1/A2 states are sampled with the first legit START condition. Once it is finished, the address is latched to minimize power dissipation associated with detection.

Table 4. P3T1750DP I2C target address table

No.	Address pin coding			Target address
	A2	A1	A0	
1	0	0	SDA	1000 000
2	0	0	SCL	1000 001
3	0	1	SDA	1000 010
4	0	1	SCL	1000 011
5	1	0	SDA	1000 100
6	1	0	SCL	1000 101
7	1	1	SDA	1000 110
8	1	1	SCL	1000 111
9	0	0	0	1001 000
10	0	0	1	1001 001

Table 4. P3T1750DP I2C target address table*...continued*

No.	Address pin coding			Target address
	A2	A1	A0	
11	0	1	0	1001 010
12	0	1	1	1001 011
13	1	0	0	1001 100
14	1	0	1	1001 101
15	1	1	0	1001 110
16	1	1	1	1001 111
17	0	SDA	SDA	1010 000
18	0	SDA	SCL	1010 001
19	0	SCL	SDA	1010 010
20	0	SCL	SCL	1010 011
21	1	SDA	SDA	1010 100
22	1	SDA	SCL	1010 101
23	1	SCL	SDA	1010 110
24	1	SCL	SCL	1010 111
25	0	SDA	0	1011 000
26	0	SDA	1	1011 001
27	0	SCL	0	1011 010
28	0	SCL	1	1011 011
29	1	SDA	0	1011 100
30	1	SDA	1	1011 101
31	1	SCL	0	1011 110
32	1	SCL	1	1011 111

7.3.2 Alert function: I2C only

The alert function is for the I2C-bus interface only. In interrupt mode (TM = 1), the ALERT pin can be connected as the SMBus alert signal. When a controller detects an alert condition on the ALERT line, the controller sends the SMBus alert command (00011001) to the bus.

If the ALERT pin is active, the device acknowledges the SMBus alert command and responds by sending its target address. The eighth bit (LSB) of the target address byte indicates whether the alert condition is caused by the temperature above T_{HIGH} or below T_{LOW}. If the temperature is higher than T_{HIGH}, the LSB bit is 1. If the temperature is lower than T_{LOW}, the LSB bit is 0.

If multiple devices respond to the alert command, arbitration during the target address portion of the alert command determines which device wins arbitration to clear alert status first. If arbitration is lost, the ALERT pin stays active.

7.3.3 General call

If the eighth bit is 0, the general call address is (0000000). The device acknowledges the general call and responds to commands in the second byte. If the second byte is 00000100, the device latches the status of the address pin. If the second byte is 00000110, the device internal registers are reset to power up values.

7.3.4 High-speed (Hs) mode

The controller device must send an I2C Hs-mode controller code (00001xxx) as the first byte after a start condition to enable the bus to high-speed operation. After the Hs-mode code is received, P3T1750DP allows I2C speed up to 3.4 MHz.

7.3.5 Timeout function

If the SDA or SCL line is held LOW for longer than t_{to} (15 ms minimum; guaranteed at 45 ms maximum), the device resets to the idle state (SDA released) and waits for a new START condition. This process ensures that the device never hangs up the bus if there are conflicts in the transmission sequence.

7.4 I3C bus serial interface

P3T1750DP interface includes a MIPI I3C SDR only target interface. The I3C controller can assign a dynamic address to P3T1750DP by issuing a SETDASA (Set Dynamic Address from Static Address) CCC command.

7.4.1 Dynamic address assigning flow

Figure 3 depicts the dynamic address assigning flowchart for P3T1750DP.

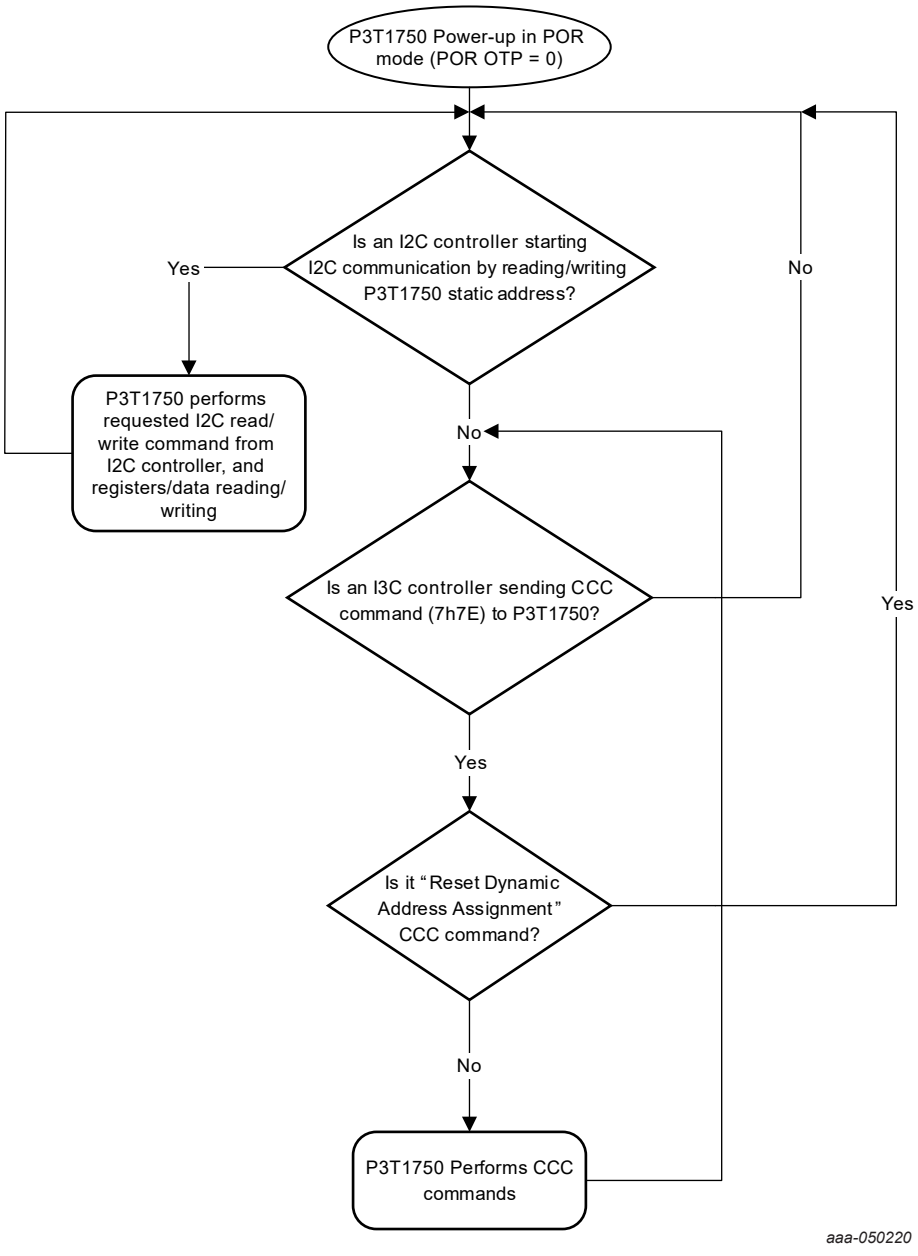


Figure 3. Dynamic address assignment flowchart

7.4.2 I3C Provisional-ID

The I3C Provisional-ID field is a 6-byte read-only (48 bits) word giving the following information:

- 15 bits with the manufacturer name, unique per manufacturer (for example, NXP).
- 1 bit indicating whether the device has a random ID or a structured Provisional-ID.
- 16 bits with the device identification, assigned by manufacturer.
- 4 bits providing the device instantiation information, for example the address pin binary input.
- 12 bits with the device revision, assigned by manufacturer.

The exact Mipi-I3C Provisional-ID composition is shown in Table 5 and Table 6 with detailed data content.

Table 5. I3C Provisional-ID composition

Manufacturer ID	Non-random part number	Device ID	Instance ID	Version
BITS[47:33]	BITS[32]	BITS[31:16]	BITS[15:12]	BITS[11:0]
15'h011B 0000 0010 0011 011	0	0001 0101 0010 1010	0000	Refer to Table 6

Table 6. I3C Provisional-ID BITS[11:0] versus I2C Address

No	I2C target address BITS[7:1]	I3C PID BITS[11:0]
1	1000 000	0000 1000 0000
2	1000 001	0000 1000 0010
3	1000 010	0000 1000 0100
4	1000 011	0000 1000 0110
5	1000 100	0000 1000 1000
6	1000 101	0000 1000 1010
7	1000 110	0000 1000 1100
8	1000 111	0000 1000 1110
9	1001 000	0000 1001 0000
10	1001 001	0000 1001 0010
11	1001 010	0000 1001 0100
12	1001 011	0000 1001 0110
13	1001 100	0000 1001 1000
14	1001 101	0000 1001 1010
15	1001 110	0000 1001 1100
16	1001 111	0000 1001 1110
17	1010 000	0000 1010 0000
18	1010 001	0000 1010 0010
19	1010 010	0000 1010 0100
20	1010 011	0000 1010 0110
21	1010 100	0000 1010 1000
22	1010 101	0000 1010 1010
23	1010 110	0000 1010 1100
24	1010 111	0000 1010 1110
25	1011 000	0000 1011 0000
26	1011 001	0000 1011 0010
27	1011 010	0000 1011 0100
28	1011 011	0000 1011 0110
29	1011 100	0000 1011 1000

Table 6. I3C Provisional-ID BITS[11:0] versus I2C Address*...continued*

No	I2C target address BITS[7:1]	I3C PID BITS[11:0]
30	1011 101	0000 1011 1010
31	1011 110[1]	0000 1011 1100
32	1011 111	0000 1011 1110

[1] The I2C address: 1011 110 (7'h 5E) doesn't support I3C SETDASA (Set Dynamic Address from Static Address) as 7'h 5E is one of I3C target-restricted addresses.

7.4.3 BCR and DCR

The I3C devices have a read-only Bus Characterization Register (BCR) and a Device Characterization Register (DCR). Both BCR and DCR can be read using the GETCBCR and GETDCR CCC.

The BCR contains information describing the role and capabilities of the device related to the I3C bus. The content of the P3T1750DP is listed in Table 7.

Table 7. Bus Characterization Register (BCR)

Bit	Function	Description
BCR[7]	Device role	2'b00: I3C target
BCR[6]		
BCR[5]	Advanced capabilities	0: Does not support optional advanced capabilities
BCR[4]	Virtual target support	0: Is not a virtual target and does not expose other downstream devices
BCR[3]	Offline capable	0: Device always reacts to I3C bus commands
BCR[2]	IBI payload	0: No data bytes follow the accepted IBI
BCR[1]	IBI request capable	1: Capable
BCR[0]	Maximum data speed limitation	1: Limitation

The DCR describes the device type for the bus controller to assess and assign the dynamic address and use common command codes as listed in Table 8.

Table 8. Device Characterization Register (DCR)

Bit [7:0]	Description
0110 0011	Temperature sensor

7.4.4 I3C Common Command Codes (CCC)

MIPI I3C devices listen to and support various common command codes (CCC) to control certain features and behaviors, such as resetting the device, enabling/disabling in-band interrupts, or renew the device dynamic address.

P3T1750DP supports CCCs that allow the controller to control multiple targets through a broadcast command at once or individual targets through direct commands listed in Table 9.

Table 9. Bus Characterization Register (BCR)

Common command code	CCC type	Command name	Default setting	Description
0x00	Broadcast	ENEC (Enable Events Command)	Enabled	Enable target event driven interrupts
0x06	Broadcast	RSTDAA (Reset Dynamic Address Assignment)	-	Forget current dynamic address and wait for a new assignment
0x07	Broadcast	ENTDAA (Enter Dynamic Address Assignment)	-	Entering controller initiation of target dynamic address assignment. Don't participate if the target already has an address assigned.
0x80	Direct	ENEC (Enable Events Command)	Enabled	Enable target event driven interrupts
0x81	Direct	DISEC (Disable Events Command)	Disabled	Disable target event driven interrupts
0x87	Direct Set	SETDASA (Set Dynamic Address from Static Address)	-	Controller assigns a dynamic address to a target with a known static address
0x88	Direct Set	SETNEWDA (Set New Dynamic Address)	-	Controller assigns a new dynamic address to any I3C target
0x8D	Direct Get	GETPID (Get Provisional ID)	-	Get the target's Provisional-ID
0x8E	Direct Get	GETBCR (Get Bus Characteristics Register)	-	Get a Device's Bus Characteristic Register (BCR)
0x8F	Direct Get	GETDCR (Get Device Characteristics Register)	-	Get a Device's Device Characteristic Register (DCR)
0x90	Direct Get	GETSTATUS (Get Device Status)	-	Get the device's operating status
0x9A	Direct	RSTACT (Target Reset Action)	-	Configure and query target reset action and timing

7.4.5 Examples of CCC protocol

7.4.5.1 ENEC/DISEC (Enable/Disable Target Events Command)

The ENEC/DISEC CCC allows the controller to control when target-initiated traffic is enabled or disabled on the I3C bus. This control governs attempts of the target to request an IBI (ENINT/DISINT) and thereby requesting controllership (ENMR/DISMR).

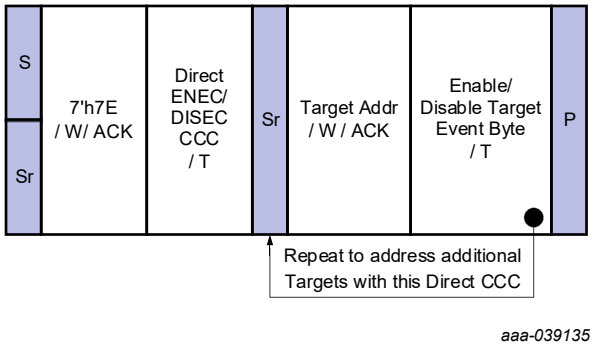


Figure 4. ENEC/DISEC format 1: Direct

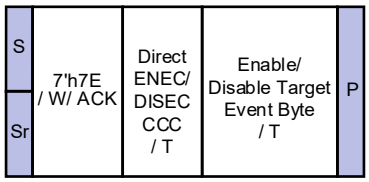


Figure 5. ENEC/DISEC format 2: Broadcast

Table 10. Enable Target Events Command byte format

Bit	7	6	5	4	3	2	1	0
Symbol	Reserved				ENHJ	Reserved	ENMR	ENINT

Table 11. Disable Target Events Command Byte Format

Bit	7	6	5	4	3	2	1	0
Symbol	Reserved				DISHJ	Reserved	DISMR	DISINT

7.4.5.2 RSTDAA (Reset Dynamic Address Assignment)

The RSTDAA broadcast CCC (Figure 6) indicates to all I3C devices that the controller requires them to clear/ reset their controller-assigned dynamic address.

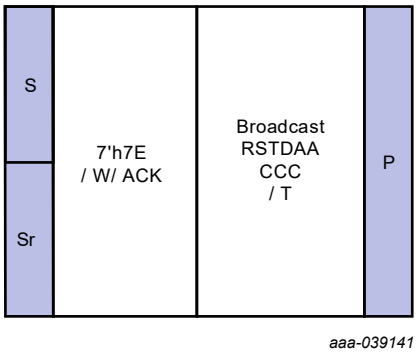


Figure 6. RSTDAA format

7.4.5.3 ENTDAA (Enter Dynamic Address Assignment)

The ENTDAA broadcast CCC (Figure 7) indicates to all I3C devices that the controller requires them to enter the dynamic address assignment procedure. Target devices that already have a dynamic address assigned do not respond to this command.

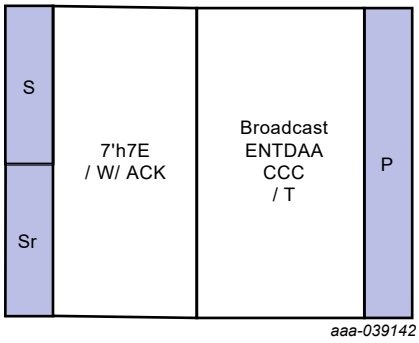


Figure 7. ENTDAA format

7.4.5.4 SETDASA (Set Dynamic Address from Static Address)

The SETDASA direct CCC (Figure 8) allows the controller to assign a dynamic address to one target using static address of the target. The SETDASA CCC must be used before the ENTDAA CCC is used.

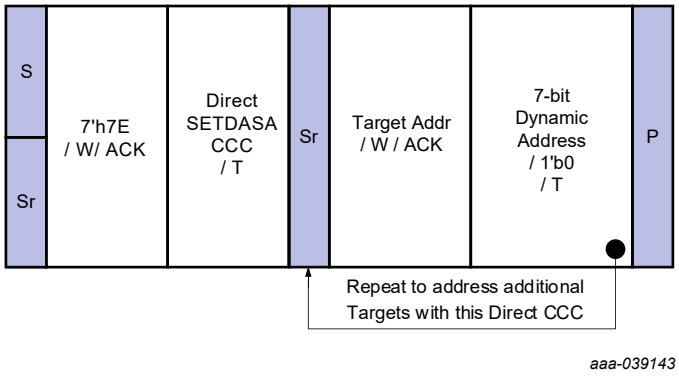


Figure 8. SETDASA format

7.4.5.5 SETNEWDA (Set New Dynamic Address)

The SETNEWDA direct CCC (Figure 9) allows the I3C controller to assign a new dynamic address to one I3C target device. In the dynamic address field, the 7 most significant bits (Bits[7:1]) contain the 7-bit dynamic address, and the least significant bit (Bit[0]) is filled with the value 1’b0.

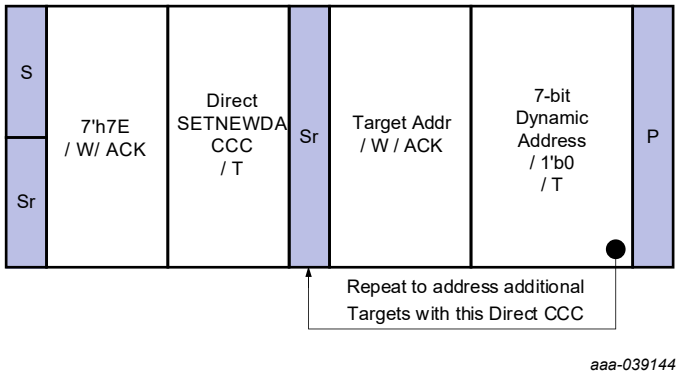


Figure 9. SETNEWDA format

7.4.5.6 GETPID (Get Provisioned-ID)

The GETPID direct CCC (Figure 10) is a get request for one I3C target device to return its 48-bit Provisioned-ID to the controller. Following transmission of the GETPID CCC, the 48-bit value is transmitted as 6 bytes, with MSB first.

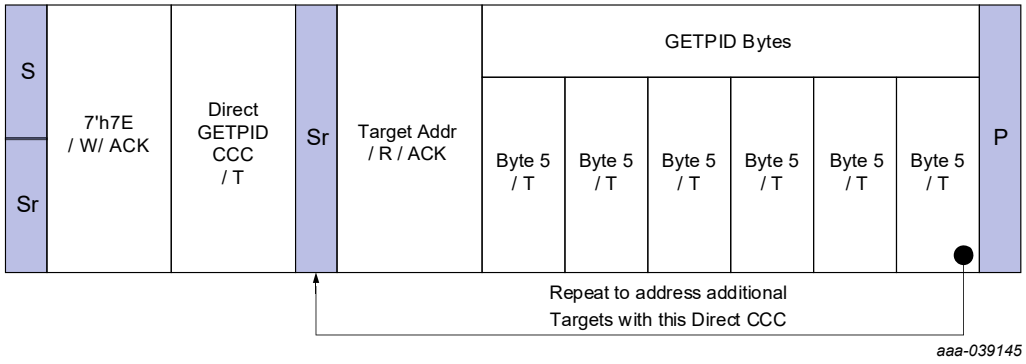


Figure 10. GETPID format

7.4.5.7 GETBCR (Get Bus Characteristics Register)

The GETBCR direct CCC (Figure 11) is a get request for one I3C target device to return its Bus Characteristics Register (BCR) to the controller. The BCR value is transmitted in one byte, with the MSB transmitted first.

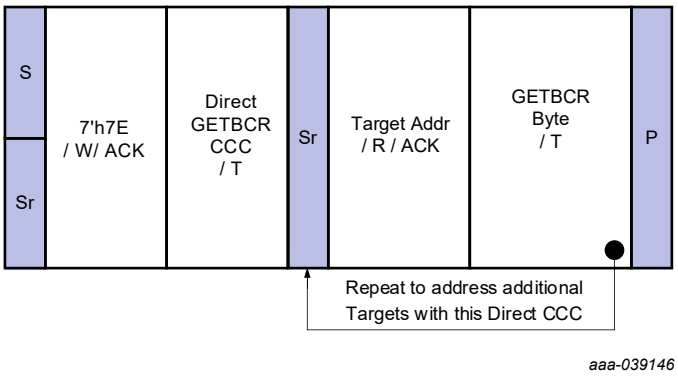


Figure 11. GETBCR format

7.4.5.8 GETDCR (Get Device Characteristics Register)

The GETDCR direct CCC (Figure 12) is a get request for one I3C target device to return its Device Characteristics Register (DCR) to the controller. The DCR value is transmitted in one byte, with the MSB transmitted first.

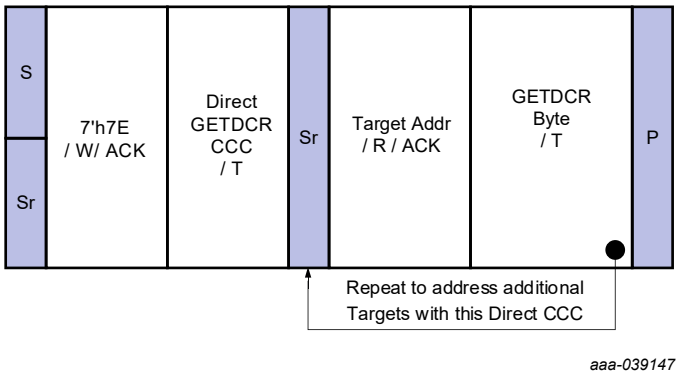


Figure 12. GETDCR format

7.4.5.9 GETSTATUS (Get Device Status)

The GETSTATUS direct CCC (Figure 13) is a get request for one I3C target device to return its current status. It returns the two-byte format detailed in Table 12.

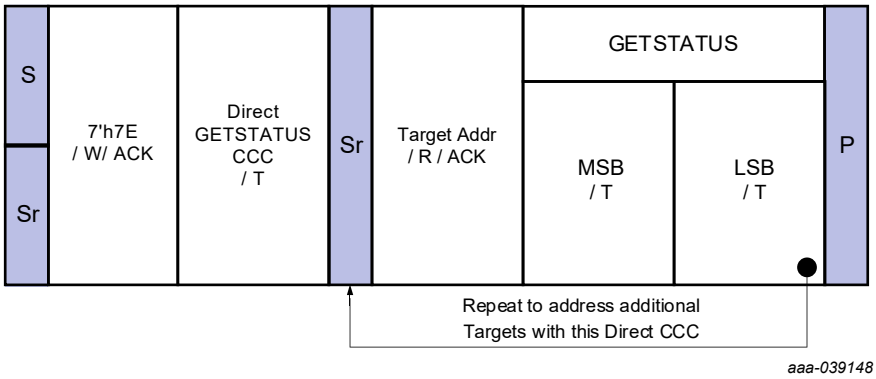


Figure 13. GETSTATUS format

Table 12. GETSTATUS MSB-LSB Format

Vendor reserved	Activity mode	Protocol error	Reserved	Pending interrupt
BITS[15:8]	BITS[7:6]	BITS[5]	BITS[4]	BITS[3:0]
0	0	0	0	0

7.4.5.10 In-Band-Interrupt (IBI)

MIPI I3C supports interrupts from target devices to controllers through the SCL/SDA 2-wire interface. The targets wait for a quiet period in which both SCL and SDA are idle and SDA is held high by a weak pullup resistor.

At least one target can pull SDA low. So, the controller is notified and starts SCL and enables the regular SDA pullup resistor to enter the address arbitration. The falling edge of SDA followed by a falling edge of SCL is then interpreted by all targets as a start condition.

Targets pulling SDA low through an open-drain driver release SDA on the falling SCL edge so it's pulled up to high through the pullup resistor.

During the following 7 SCL pulses all eligible targets can transmit their dynamic address to the controller. The lowest dynamic address is recognized as the one with the highest priority. Once a target determines that

another target is driving a lower address through its open-drain output on SDA, it refrains from interfering with any further communication on SDA while the current communication continues.

The 7 address bits are followed by RnW = 1 and an ACK driven by the controller (if the controller acknowledges).

7.5 Register list

The P3T1750DP contains four data registers beside the pointer register as listed in Table 13, the pointer value, read/write capability, and default content at power up of the registers.

Table 13. Register table

Register name	Pointer value	R/W	POR state	Description
Temp	00h	Read only	0000h	Temperature register: contains two 8-bit data bytes; to store the measured Temp data.
Conf	01h	R/W	28h	Configuration register: contains a single 8-bit data byte; to set the device operating condition.
T_{LOW}	02h	R/W	4B00h	T_{LOW} register: Hysteresis register, it contains two 8-bit data bytes to store the hysteresis T_{LOW} limit; default = 75 °C.
T_{HIGH}	03h	R/W	5000h	T_{HIGH} register: Overtemperature shut down threshold register, it contains two 8-bit data bytes to store the overtemperature shutdown T_{HIGH} limit; default = 80 °C.

7.5.1 Pointer register

The pointer register contains an 8-bit data byte, of which the two LSB bits represent the pointer bits of the other four registers, and the other 6 MSB bits are equal to 0, as shown in Table 14 and Table 15. The pointer register is not accessible to the user, but is used to select the data register for write/read operation by including the pointer data byte in the bus command.

Table 14. Pointer register

B7	B6	B5	B4	B3	B2	B[1:0]
0	0	0	0	0	0	Pointer Bits

Table 15. Pointer addresses

B1	B0	Selected register
0	0	Temperature register (Temp, read only)
0	1	Configuration register (read/write)
1	0	T_{LOW} register (read/write)
1	1	T_{HIGH} register (read/write)

The pointer value is latched into the pointer register when the bus command (which includes the pointer byte) is executed. Therefore, a read from the P3T1750DP either includes the pointer byte in the statement or excludes it. To read a register again that has been recently read and the pointer has been preset, the pointer byte does not have to be included. To read a register that is different from the one that has been recently read, the pointer byte must be included. However, a write to the device must always include the pointer byte in the statement. Section 7.6 describes the bus communication protocols.

At power up, the pointer value is equal to 000b and the Temp register is selected. Users can then read the Temp data without specifying the pointer byte.

Anything not shown in Table 15 is reserved and must not be used.

7.5.2 Temperature register

The temperature register (Temp) holds the digital result of temperature measurement or monitor at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes consisting of one most significant byte (MSByte) and one least significant byte (LSByte). However, only 12 bits of those two bytes are used to store the Temp data in two's complement format with the resolution of 0.0625 °C. Table 16 and Table 17 show the bit arrangement of the Temp data in the data bytes.

After power up or reset value, the temperature register default value reads 0 °C. The value is updated after completing the first conversion.

Table 16. Temperature register - Byte 1

D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4

Table 17. Temperature register - Byte 2

D7	D6	D5	D4	D3	D2	D1	D0
T3	T2	T1	T0	0	0	0	0

When reading register Temp, all 16 bits of the two data bytes (MSByte and LSByte) are provided to the bus and the controller must collect these bits for a valid temperature reading. However, only the 12 most significant bits must be used, and the four least significant bits of the LSByte are zero and must be ignored. One of the ways to calculate the Temp value in °C from the 12-bit Temp data is:

1. If the Temp data MSByte bit T11 = 0, then the temperature is positive and the Temp value (°C) = +(Temp data) x 0.0625 °C.
   Example: 0100 1011 0000 = 4B0h = 1200. ≥ Temp = 1200 x 0.0625 °C. = +75 °C
2. If the Temp data MSByte bit T11 = 1, then the temperature is negative.
   Temp value (°C) = -(two's complement of Temp data and adding one) x 0.0625 °C
   Example: 1110 0111 000:
   Two's complement and adding one: 0001 1000 1111+1 = 0001 1001 0000 = 190h = 400
   Temp = - 400 x 0.0625 °C = -25 °C

Examples of the Temp data and value are shown in Table 18.

Table 18. Temp register value

Temperature (°C)	ADC value	
	Binary	Hex
127.9375	0111 1111 1111	7FF
127	0111 1111 0000	7F0
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320

Table 18. Temp register value*...continued*

Temperature (°C)	ADC value	
	Binary	Hex
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
-0.25	1111 1111 1100	FFC
-25	1110 0111 0000	E70
-40	1101 1000 0000	D80

7.5.3 Configuration register

The configuration register (Conf) is a write/read register and contains an 8-bit non-complement data byte that is used to configure the device for different operating conditions. Table 19 shows the bit assignments of this register.

Table 19. Configuration register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	OS	R1	R0	F1	F0	POL	TM	SD

7.5.4 Shutdown mode (SD)

The shutdown mode can reduce power dissipation by shutting down all circuitry other than the I2C/I3C interface; current consumption is around 0.2 µA typically. Shutdown mode is set by SD bit = 1; the device shuts down when the current conversion is completed. When SD = 0, the temperature sensor is in a continuous conversion state.

7.5.5 Thermostat mode (TM)

The P3T1750DP thermostat mode (TM) bit shows that the device is in interrupt mode (TM = 1) or comparator mode (TM = 0, default). See Section 7.5.10.

7.5.6 Polarity (POL)

The polarity bit can adjust the polarity of the ALERT pin output. When the POL bit is set to 0 (default value), the ALERT pin becomes active low. When the POL bit is 1, the ALERT pin becomes active high and the state of the ALERT pin is reversed.

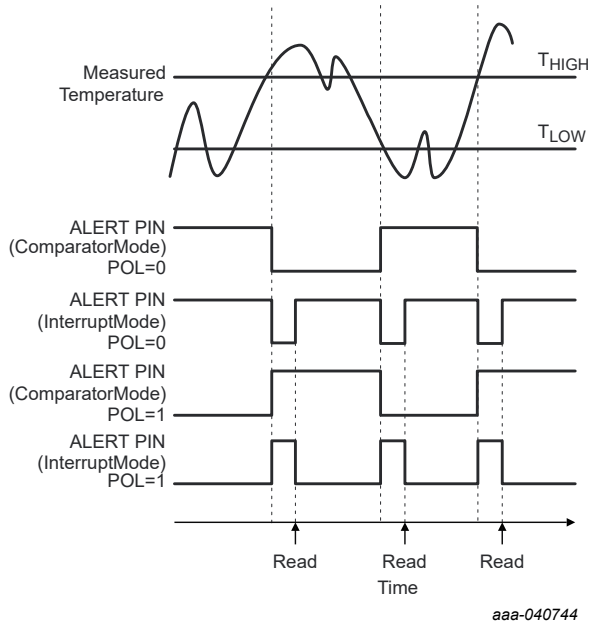


Figure 14. ALERT pin and POL diagram

7.5.7 Fault queue (F1/F0)

When the measured temperature exceeds the user-defined limit set in the T_{HIGH} and T_{LOW} registers, the fault condition is triggered. The fault queue can be programmed for the number of fault conditions required to generate an alert to prevent a false alert caused by environmental noise. Table 20 defines the number of measured faults that can be set to trigger an alert condition in the temperature sensor. See the Section 7.5.10 section T_{HIGH} and T_{LOW} registers format.

Table 20. Fault settings

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2 (default)
1	0	4
1	1	6

7.5.8 Conversion time (R1 and R0)

Bits R1 and R0 determine the converter time. Table 21 identifies the resolution bits and the conversion time.

Table 21. Conversion time

R1	R0	Conversion time
0	0	27.5 ms
0	1	55 ms (default)
1	0	110 ms
1	1	220 ms

7.5.9 One-Shot (OS)

P3T1750DP has a one-shot temperature measurement mode. When P3T1750DP is set in shutdown mode, writing 1 to the OS bit starts the one-shot temperature measurement (that is, single temperature conversion.) After the conversion is complete, P3T1750DP returns to the shutdown state. When continuous temperature monitoring is not required, this function can be used to reduce the power consumption of the P3T1750DP. When reading the configuration register, the OS always reads zero.

7.5.10 High and low-limit registers

In the comparator mode (TM = 0), when the temperature equals or exceeds the value in T_{HIGH}, the ALERT pin becomes active, and a consecutive number of faults are generated according to the fault bits F1 and F0. The ALERT pin remains active until the temperature drops below the indicated T_{LOW} value for the same consecutive number of faults.

In interrupt mode (TM = 1), when the temperature equals or exceeds T_{HIGH} for a consecutive number of fault conditions, the ALERT pin becomes active. The ALERT pin remains active until any register read operation occurs or the device responds to the SMBus Alert response address successfully. If the device is set in shutdown mode, the ALERT pin is also cleared. After the ALERT pin is cleared, the pin becomes active again only when the temperature drops below T_{LOW}. When the temperature drops below T_{LOW}, the ALERT pin becomes active and remains active until any register read operation clears it, or the device responds to the SMBus Alert response address successfully. After the ALERT pin is cleared, the above cycle is repeated, and the ALERT pin becomes active when the temperature equals or exceeds T_{HIGH}. The ALERT pin can also be cleared by resetting the device using the general call reset command. By returning the device to the comparator mode (TM = 0), this operation also clears the state of the internal registers in the device.

Table 22, Table 23, Table 24, and Table 25 describe the format of the T_{HIGH} and T_{LOW} registers. The most significant byte is sent first, and then the least significant byte. The power-on reset values of T_{HIGH} and T_{LOW} are:

T_{HIGH} = 80 °C and T_{LOW} = 75 °C

The data format of T_{HIGH} and T_{LOW} is the same as the temperature register.

Table 22. Byte 1 of the T_{HIGH} register

D7	D6	D5	D4	D3	D2	D1	D0
H11	H10	H9	H8	H7	H6	H5	H4

Table 23. Byte 2 of the T_{HIGH} register

D7	D6	D5	D4	D3	D2	D1	D0
H3	H2	H1	H0	0	0	0	0

Table 24. Byte 1 of the T_{LOW} register

D7	D6	D5	D4	D3	D2	D1	D0
L11	L10	L9	L8	L7	L6	L5	L4

Table 25. Byte 2 of the T_{LOW} register

D7	D6	D5	D4	D3	D2	D1	D0
L3	L2	L1	L0	0	0	0	0

7.6 Protocols for writing and reading the registers

The communication between the host and the device must strictly follow the rules as defined by the I2C-bus management. The protocols for device register read/write operations are illustrated in Figure 15 to Figure 20 together with the following definitions:

1. Before a communication, the I2C-bus must be free or not busy. It means that all devices on the bus must release both SCL and SDA lines, and they become HIGH by the bus pullup resistors.
2. The host must provide the SCL clock pulses necessary for the communication. Data is transferred in a sequence of 9 SCL clock pulses for every 8-bit data byte, followed by the 1-bit status of the acknowledgment.
3. During data transfer, except the START and STOP signals, the SDA signal must be stable while the SCL signal is HIGH. It means that the SDA signal can be changed only during the LOW duration of the SCL line.
4. S: START signal, initiated by the host to start a communication, the SDA goes from HIGH to LOW while the SCL is HIGH.
5. RS: RE-START signal, same as the START signal, to start a read command that follows a write command.
6. P: The STOP signal, generated by the host to stop a communication, the SDA goes from LOW to HIGH while the SCL is HIGH. The bus becomes free thereafter.
7. W: Write bit, when the write/read bit = LOW in a write command.
8. R: Read bit, when the write/read bit = HIGH in a read command.
9. A: Device acknowledge bit returned by the device. It is LOW if the device works properly and HIGH if not. The host must release the SDA line during this period to give the device the control on the SDA line.
10. A': Controller acknowledge bit, not returned by the device, but set by the controller or host in reading 2-byte data. During this clock period, the host must set the SDA line to LOW to notify the device that the first byte has been read for the device to provide the second byte onto the bus.
11. NA: Not Acknowledge bit. During this clock period, both the device and host release the SDA line at the end of a data transfer, the host is then enabled to generate the STOP signal.
12. In a write protocol, data is sent from the host to the device and the host controls the SDA line, except during the clock period when the device sends the device acknowledgment signal to the bus.
13. In a read protocol, the device sends data to the bus and the host must release the SDA line while the device is providing data onto the bus and controlling the SDA line, except during the clock period when the controller sends the controller acknowledgment signal to the bus.
14. For best temperature accuracy, both temperature bytes must be read as shown in Figure 19 and Figure 20. But for a quick less accurate check/reduce bus transmission, only one byte, the MSByte, must be read as shown in Figure 20.

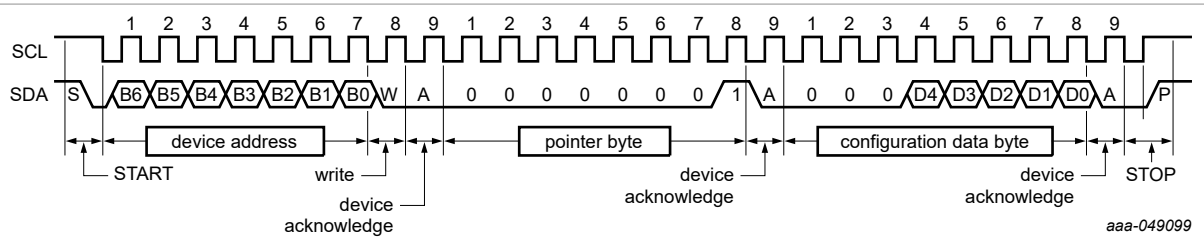


Figure 15. Write configuration register (1-byte data)

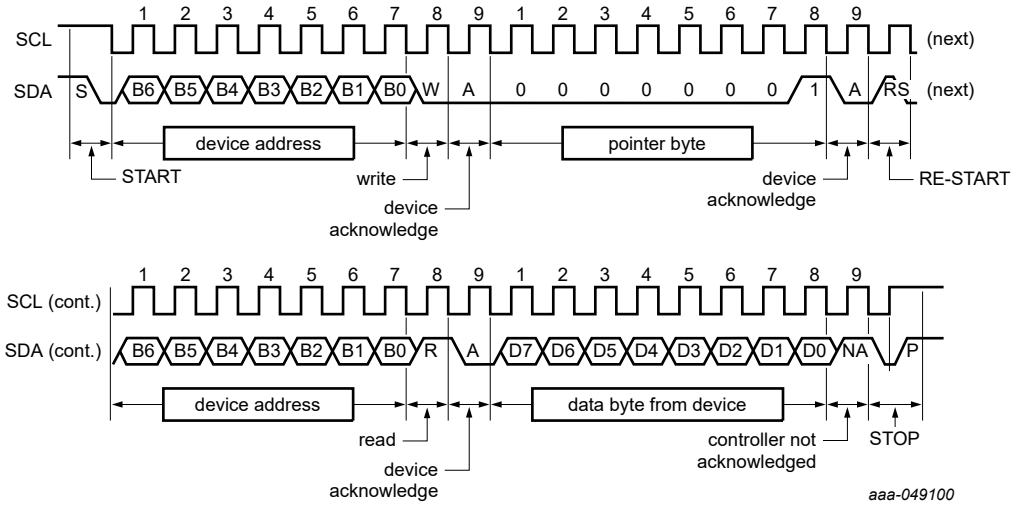


Figure 16. Read configuration register including pointer byte (1-byte data)

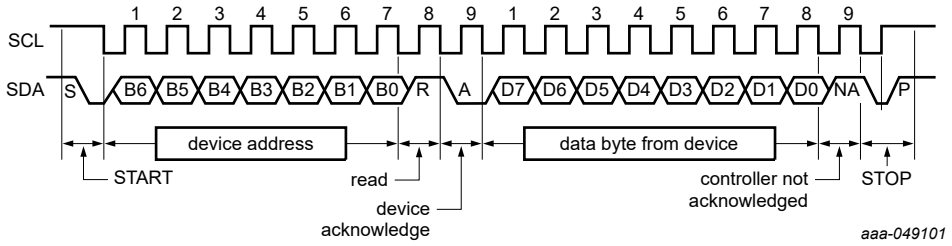


Figure 17. Read configuration or temp register with preset pointer (1-byte data)

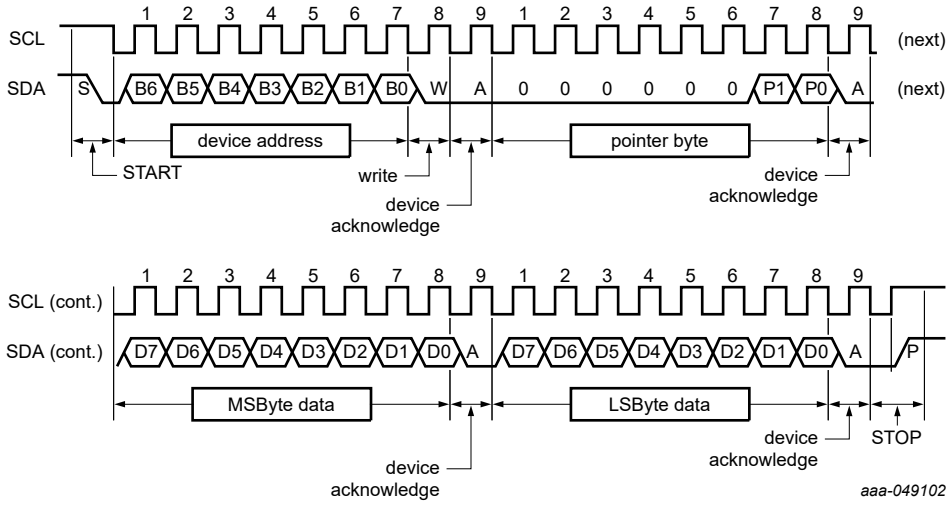


Figure 18. Write register (2-byte data)

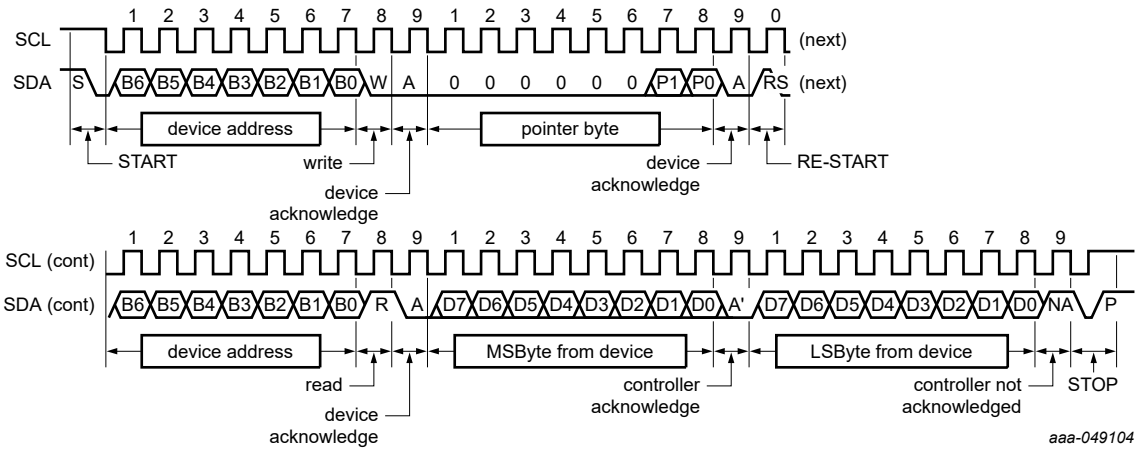


Figure 19. Read register including pointer byte (2-byte data)

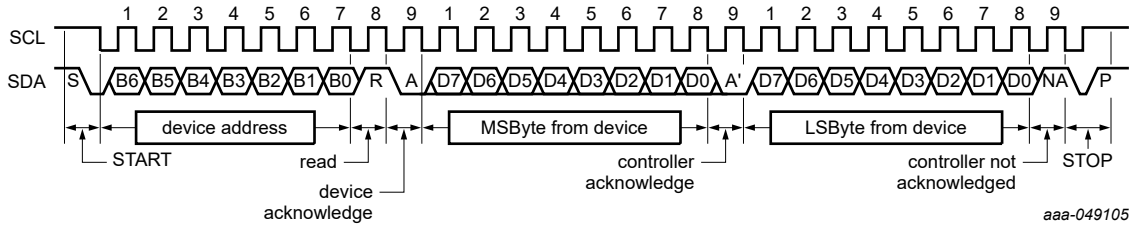
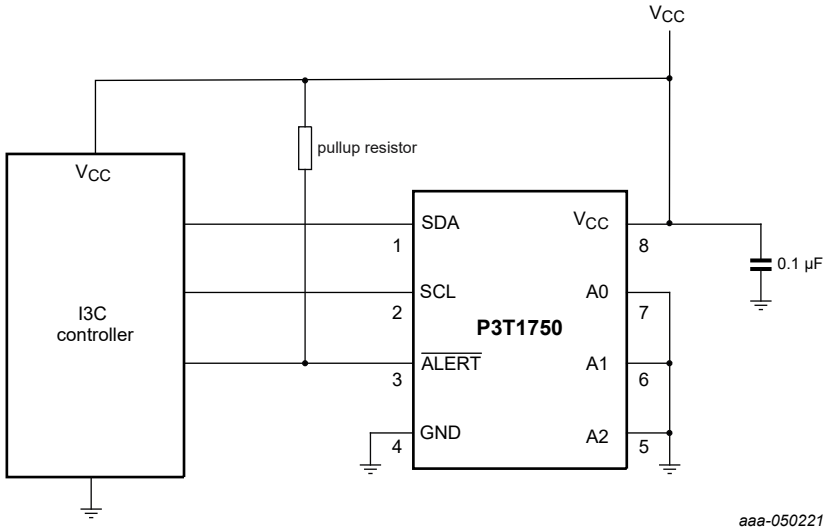


Figure 20. Read register with preset pointer (2-byte data)

8 Application design-in information

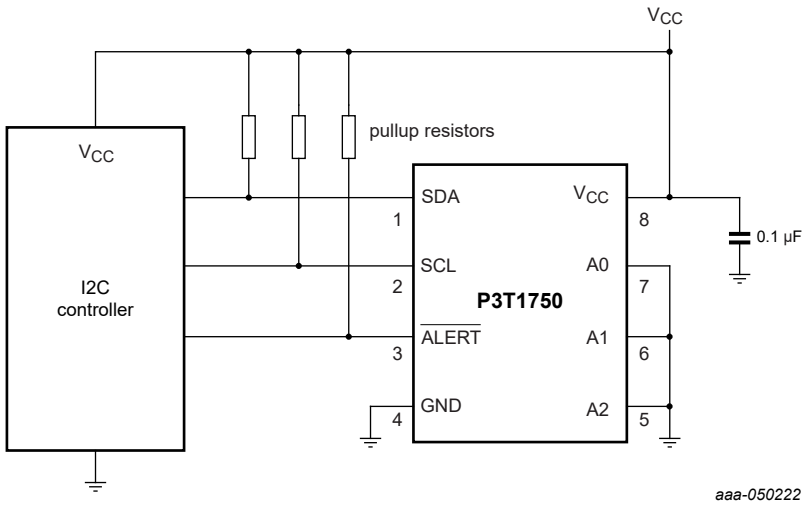
8.1 Typical application

Figure 21 and Figure 22 depict the I3C and I2C typical application, respectively.



See Section 7.3.1 and Section 7.4.2 for A0, A1, and A2 configuration.

Figure 21. I3C typical application



See Section 7.3.1 and Section 7.4.2 for A0, A1, and A2 configuration.

Figure 22. I2C typical application

8.2 Temperature accuracy

The local channel of the temperature sensor measures its own die temperature that is transferred from its body. Therefore, the temperature of the device body must be stabilized and saturated for it to provide the stable readings. Because the device operates at a low-power level, the thermal gradient of the device package has a minor effect on the measurement.

The accuracy of the measurement is more dependent upon the definition of the environment temperature. The printed-circuit board on which the device is mounted and the air flow contacting the device body affects the

environmental temperature. If the ambient air temperature and the printed-circuit board temperature are much different, then the measurement cannot be stable because of the different thermal paths between the die and the environment.

The stabilized temperature liquid of a thermal bath provides the best temperature environment when the device is dipped into it. A thermal probe with a device mounted inside a sealed-end metal tube is located in consistent temperature air, which provides a good method of temperature measurement.

8.3 Noise effect

The device design includes the implementation of basic features for a good noise immunity:

- The 20 ns low-pass filter on both the bus pins SCL and SDA.
- The hysteresis of the threshold voltages to the bus input signals SCL and SDA, about 200 mV minimum.

However, good layout practices and extra noise filters are recommended when the device is used in a noisy environment:

- Use decoupling capacitors at V_{CC} pin.
- Keep the digital traces away from switching power supplies.
- Apply proper terminations for the long board traces.
- Add capacitors to the SCL and SDA lines, which increase the low-pass filter characteristics.

8.4 POR and I3C communication

To execute the power-on reset (POR) successfully and ensure normal operation, V_{CC} requires a starting voltage that is less than 300 mV. If this rule is violated, the device can remain in an indeterminate state that causes I2C/I3C communication failure.

9 Limiting values

Table 26 describes the limiting values of P3T1750DP.

Table 26. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		-0.3	+4.0	V
V_I	Input voltage	SCL, A0, A1, and A2 at V_{CC} = -0.3 V to +4 V	-0.3	+4.0	V
		SDA, ALERT at V_{CC} = +1.4 V to +4 V	-0.3	V_{CC} + 0.3 V and ≤ 4 V	V
		SDA, ALERT at V_{CC} = +0 V	-0.3	+4.0	V
I_I	Input current	At input pins	-5.0	+5.0	mA
V_o	Output voltage	At output pin	-0.3	+4.0	V
T_{op}	Operating temperature		−40	+125	°C
T_{stg}	Storage temperature		-65	+150	°C
T_j	Junction temperature		-	150	°C
V_{ESD}	Electrostatic discharge voltage	Human body model (HBM) JS-001-2017; all pins	-2000	+2000	V
		Charge device model (CDM) JS-002-2018; all pins	-1000	+1000	V

9.1 Thermal characteristics

Table 27 provides the thermal characteristics of P3T1750DP.

Table 27. P3T1750DP (TSSOP8) thermal characteristics

Symbol	Parameter	Value (typ)[1]	Unit
θJA	Junction-to-ambient thermal resistance	190	°C/W
θJC(top)	Junction-to-case(top) thermal resistance	81	°C/W
θJB	Junction-to-board thermal resistance	110	°C/W
ΨJT	Junction-to-top characterization parameter	16.1	°C/W
ΨJB	Junction-to-board characterization parameter	112.5	°C/W

[1] P3T1750DP power dissipation is less than 1 mW. (See Table 26 for IQ versus different conditions.) The self-heating is neglectable.

10 Recommended operating conditions

Table 28 describes the recommended operation conditions for P3T1750DP.

Table 28. Recommended operating characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply voltage		1.4	-	3.6	V
V_I	Input voltage	SCL, A0, A1, and A2	0	-	3.6	V
		SDA, ALERT at V_{CC} = +1.4 V to +3.6 V			V_{CC} + 0.3 and ≤ 3.6	V
		SDA, ALERT at V_{CC} = +0 V	0		3.6[1]	V
V_O	Output voltage	Digital pins	0		V_{CC}[2]	V
T_{amb}	Ambient temperature		-40	-	+125	°C

[1] It allows the system to turn off P3T1750DP V_{CC} and keeps I2C/I3C bus V_{CC} active for power management.
[2] For push-pull, the V_O max = V_{CC}. For open-drain, the pullup V_O max = 3.6 V.

11 Static characteristics

This section describes the static characteristics of P3T1750DP.

Table 29. Static characteristics

V_{CC} = 1.4 V to 3.6 V; T_{amb} = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{acc}	Temperature accuracy	T = -40 °C to + 125 °C, 1.4 V ≤ V_{CC} ≤ 3.6 V	-1	-	+1	°C
T_{res}	Temperature resolution	12-bit digital temp data	-	0.0625	-	°C

Table 29. Static characteristics...*continued*

V_{CC} = 1.4 V to 3.6 V; T_{amb} = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$t_{conv(T)}$	Temperature conversion time	One-shot mode		7.8	12	ms
Con_{MOD}	Conversion modes	R1 = 0, R0 = 0		27.5		ms
		R1 = 0, R0 = 1 (default)		55		ms
		R1 = 1, R0 = 0		110		ms
		R1 = 1, R0 = 1		220		ms
V_{POR}	Power-on reset voltage	V_{CC} must ramp up from initial level <300 mV	-	-	1.2	V
t_{act}	Active time	I2C/I3C active after $V_{CC} \geq V_{POR}$	-	-	20	ms
I_Q	Quiescent current (V_{CC} = 1.8 V)	I2C bus inactive, R1 = 1, R0 = 1, T_{amb} = +25 °C		4.1	6.3	µA
		I2C bus inactive, R1 = 1, R0 = 1, -40 °C to +125 °C			19.2	µA
		I2C bus active, SCL frequency = 400 kHz, R1 = 1, R0 = 1		10		µA
		I2C bus active, SCL frequency = 3.4 MHz, R1 = 1, R0 = 1		80		µA
I_{SD}	Shutdown current (V_{CC} = 1.8 V)	I2C bus inactive, T_{amb} = +25 °C		0.2	1	µA
		I2C bus active, SCL frequency = 400 kHz		8		µA
		I2C bus active, SCL frequency = 3.4 MHz		75		µA
V_{IH}	HIGH-level input voltage	Digital pins (SCL, SDA, and A0)	0.7 x V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	Digital pins	-	-	0.3 x V_{CC}	V
I_{IN}	Digital pin input current	0 V < V_{IN}< V_{CC} + 0.3 at T_{amb} = 25 °C	-		1	µA
V_{OL}	LOW-level output voltage	V_{CC} > 2 V; I_{OL} = 3 mA	-	-	0.4	V
		V_{CC} < 2 V; I_{OL} = 3 mA	-	-	0.2 x V_{CC}	V
C_I	Input capacitance	Digital pins	-	-	10	pF

[1] Typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

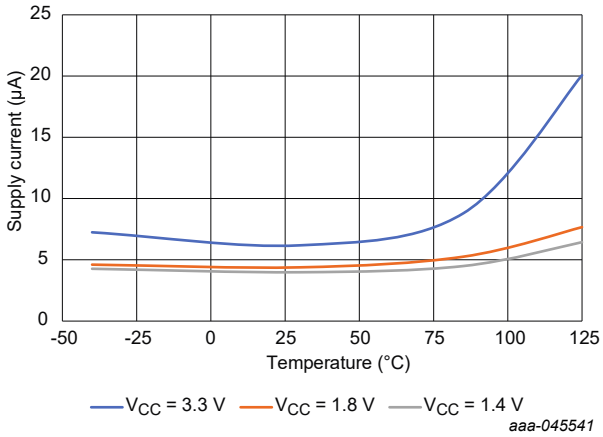


Figure 23. Supply current versus temperature (bus inactive, one conversion per second)

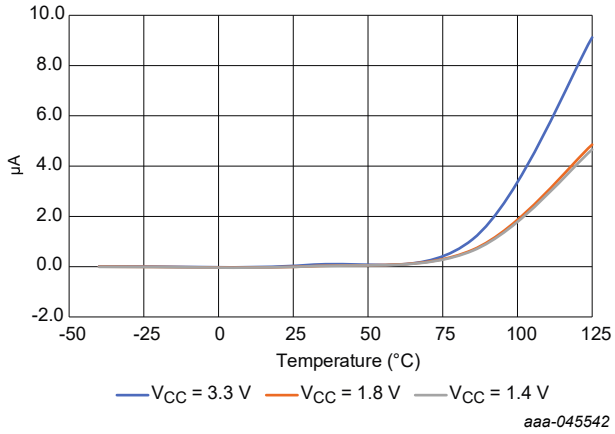


Figure 24. Shutdown current versus temperature

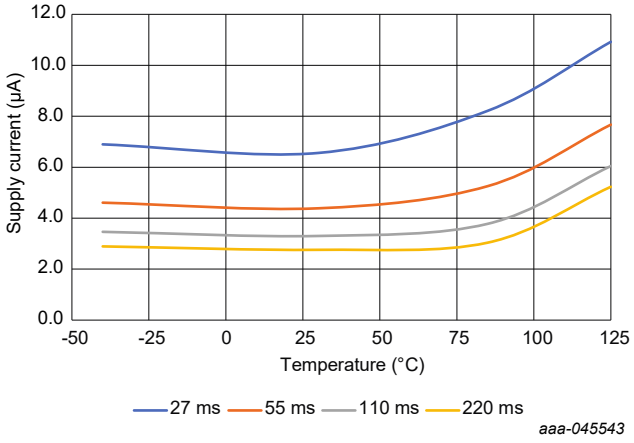


Figure 25. Supply current versus conversion time and temperature (V_{CC} = 1.8 V, bus inactive)

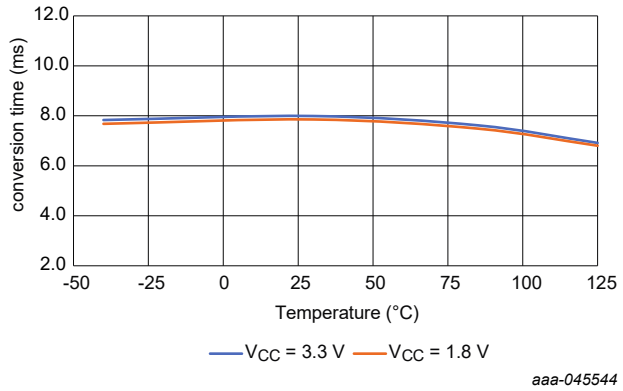


Figure 26. One-shot conversion time versus temperature

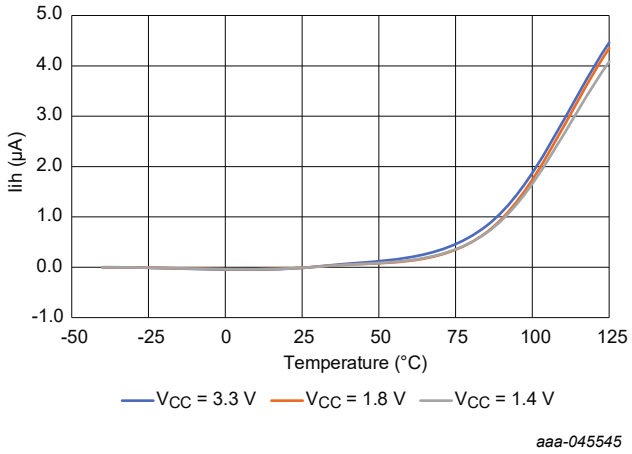


Figure 27. HIGH-level input current versus temperature; digital pins (V_{CC} = 1.4 V to 3.6 V)

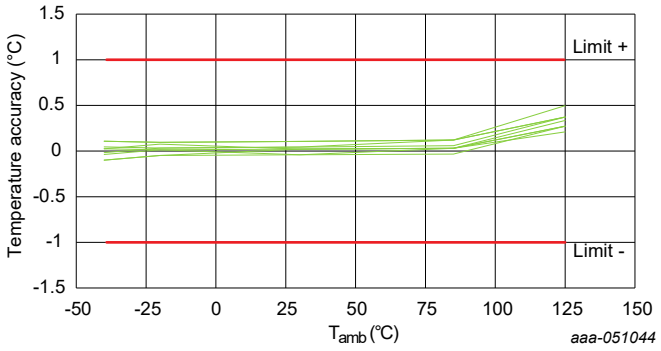


Figure 28. Accuracy versus temperature (V_{CC} = 1.4 V to 3.6 V)

12 Dynamic characteristics

This section describes the dynamic characteristics of P3T1750DP.

Table 30. I2C-bus interface dynamic characteristics

V_{CC} = 1.4 V to 3.6 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified. These specifications are guaranteed by design and not tested in production.

Symbol	Parameter	Conditions	Fast Mode		High-speed mode		Unit
			Min	Max	Min	Max	
fSCL	SCL clock frequency, V_{CC} ≥ 1.8 V		0.001	0.4	0.001	3.4	MHz
	SCL clock frequency, V_{CC} < 1.8 V		0.001	0.4	0.001	2.5	MHz
t_{HIGH}	HIGH period of the SCL clock		600	-	60	-	ns
t_{LOW}	LOW period of the SCL clock, V_{CC} ≥ 1.8 V		1300	-	160	-	ns
	LOW period of the SCL clock, V_{CC} < 1.8 V		1300	-	260	-	ns
$t_{HD;STA}$	Hold time (repeated) START condition		600	-	160	-	ns
$t_{SU;DAT}$	Data set-up time, V_{CC} ≥ 1.8 V		100	-	10	-	ns
	Data set-up time, V_{CC} < 1.8 V		100	-	45	-	ns
$t_{HD;DAT}$	Data hold time, V_{CC} ≥ 1.8 V		20	900	20	70	ns
	Data hold time, V_{CC} < 1.8 V		20	900	20	130	ns
$t_{SU;STO}$	Set-up time for STOP condition		0.6	-	0.16	-	µs
t_r, $t_{f(SCL)}$	Clock rise/fall time		-	300	-	40	ns
t_r, $t_{f(SDA)}$	Data rise/fall time		-	300	-	80	ns
t_r	Clock/data rise time for SCL ≤ 100 kHz	SCL ≤ 100 kHz	-	1000	-	-	ns

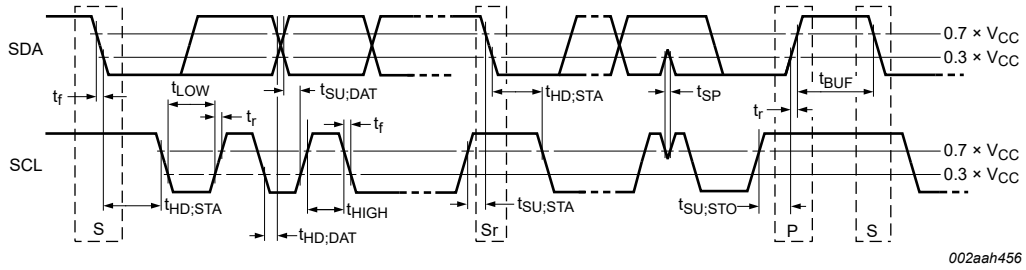


Figure 29. Timing diagram

Table 31. I3C bus interface dynamic characteristics

V_{CC} = 1.4 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified. These specifications are guaranteed by design and not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
I3C open-drain timing parameters					
t_{HIGH}	HIGH period of the SCL clock			41	ns
t_{LOW_OD}	LOW period of the SCL clock	200		-	ns
t_{DIG_H}	Logic HIGH period of the SCL clock	32		t_{HIGH} + t_{CF}	ns
$t_{DIG\_OD\_L}$	Logic LOW period of the SCL clock	t_{LOW_ODmin} + t_{fDA_ODmin}			ns

Table 31. I3C bus interface dynamic characteristics...*continued*

V_{CC} = 1.4 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified. These specifications are guaranteed by design and not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
t_{fDA_OD}	Fall time of SDA	t_{CF}		21	ns
t_{SU_OD}	SDA setup time during open-drain mode	3			ns
t_{CAS}	Clock after Start condition	38.4n			s
t_{CBP}	Clock before Stop condition	$t_{CASmin/2}$			s
$t_{MMoverlap}$	Current controller to secondary controller overlap time during handoff	$t_{DIG\_OD\_Lmin}$			ns
t_{AVAL}	Bus available condition	20			µs
t_{IDLE}	Bus idle condition	1			ms
t_{MMLock}	Time internal where the new controller is not driving SDA low	$t_{AVALmin}$			µs
I3C push_pull timing parameters					
f_{SCL}	SCL clock frequency	0.01	9.8	10	MHz
t_{HIGH}	HIGH period of the SCL clock	24		-	ns
t_{LOW}	LOW period of the SCL clock	57		-	ns
t_{DIG_H}	Logic HIGH period of the SCL clock	32		-	ns
t_{DIG_L}	Logic LOW period of the SCL clock	65		-	ns
$t_{DIG\_H\_MIXED}$	Logic HIGH period of the SCL clock for mixed bus	32		-	ns
t_{HIGH_MIXED}	HIGH period of the SCL clock for mixed bus	24		-	ns
t_{SCO}	Clock in to data out for target			42	ns
t_{CR}	Fall time of SCL signal	-	$150/f_{SCL}$		ns
t_{CF}	Fall time of SCL signal	-	$150/f_{SCL}$		ns
t_{HD_PP}	SDA signal data hold in push-pull mode	0		-	ns
t_{SU_PP}	SDA signal data set up in push-pull mode	3		-	ns
t_{CASr}	Clock after repeated Start (Sr)	t_{CASmin}		-	ns
t_{CBSr}	Clock before repeated Start (Sr)	$t_{CASmin}/2$		-	ns
C_b	Capacitive load per bus line (SCL/SDA)	-		50	pF

Table 32. I3C bus interface dynamic characteristics

V_{CC} = 1.8 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified. These specifications are guaranteed by design and not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
I3C open-drain timing parameters					
t_{HIGH}	HIGH period of the SCL clock			41	ns
t_{LOW_OD}	LOW period of the SCL clock	200		-	ns
t_{DIG_H}	Logic HIGH period of the SCL clock	32		$t_{HIGH} + t_{CF}$	ns

Table 32. I3C bus interface dynamic characteristics...*continued*

V_{CC} = 1.8 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified. These specifications are guaranteed by design and not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{DIG\_OD\_L}$	Logic LOW period of the SCL clock	t_{LOW_ODmin} + t_{fDA_ODmin}			ns
t_{fDA_OD}	Fall time of SDA	t_{CF}		16	ns
t_{SU_OD}	SDA setup time during open-drain mode	3			ns
t_{CAS}	Clock after Start condition	38.4n			s
t_{CBP}	Clock before Stop condition	$t_{CASmin/2}$			s
$t_{MMoverlap}$	Current controller to secondary controller overlap time during handoff	$t_{DIG\_OD\_Lmin}$			ns
t_{AVAL}	Bus available condition	20			µs
t_{IDLE}	Bus idle condition	1			ms
t_{MMLock}	Time internal where the new controller is not driving SDA low	$t_{AVALmin}$			µs
I3C push_pull timing parameters					
f_{SCL}	SCL clock frequency	0.01	12.5	12.9	MHz
t_{HIGH}	HIGH period of the SCL clock	24		-	ns
t_{LOW}	LOW period of the SCL clock	38		-	ns
t_{DIG_H}	Logic HIGH period of the SCL clock	32		-	ns
t_{DIG_L}	Logic LOW period of the SCL clock	32		-	ns
$t_{DIG\_H\_MIXED}$	Logic HIGH period of the SCL clock for mixed bus	32		-	ns
t_{HIGH_MIXED}	HIGH period of the SCL clock for mixed bus	24		-	ns
t_{SCO}	Clock in to data out for target			28	ns
t_{CR}	Fall time of SCL signal	-	$150/f_{SCL}$		ns
t_{CF}	Fall time of SCL signal	-	$150/f_{SCL}$		ns
t_{HD_PP}	SDA signal data hold in push-pull mode	0		-	ns
t_{SU_PP}	SDA signal data set up in push-pull mode	3		-	ns
t_{CASr}	Clock after repeated Start (Sr)	t_{CASmin}		-	ns
t_{CBSr}	Clock before repeated Start (Sr)	$t_{CASmin}/2$		-	ns
C_b	Capacitive load per bus line (SCL/SDA)	-		50	pF

Table 33. I3C bus interface dynamic characteristics

V_{CC} = 3.6 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified. These specifications are guaranteed by design and not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
I3C open-drain timing parameters					
t_{HIGH}	HIGH period of the SCL clock			41	ns
t_{LOW_OD}	LOW period of the SCL clock	200		-	ns

Table 33. I3C bus interface dynamic characteristics...*continued*

V_{CC} = 3.6 V; T_{amb} = −40 °C to +125 °C; unless otherwise specified. These specifications are guaranteed by design and not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
t_{DIG_H}	Logic HIGH period of the SCL clock	32		t_{HIGH} + t_{CF}	ns
$t_{DIG\_OD\_L}$	Logic LOW period of the SCL clock	t_{LOW_ODmin} + t_{fDA_ODmin}			ns
t_{fDA_OD}	Fall time of SDA	t_{CF}		12	ns
t_{SU_OD}	SDA setup time during open-drain mode	3			ns
t_{CAS}	Clock after Start condition	38.4n			s
t_{CBP}	Clock before Stop condition	$t_{CASmin/2}$			s
$t_{MMoverlap}$	Current controller to secondary controller overlap time during handoff	$t_{DIG\_OD\_Lmin}$			ns
t_{AVAL}	Bus available condition	20			µs
t_{IDLE}	Bus idle condition	1			ms
t_{MMLock}	Time internal where the new controller is not driving SDA low	$t_{AVALmin}$			µs
I3C push_pull timing parameters					
f_{SCL}	SCL clock frequency	0.01	12.5	12.9	MHz
t_{HIGH}	HIGH period of the SCL clock	24		-	ns
t_{LOW}	LOW period of the SCL clock	24		-	ns
t_{DIG_H}	Logic HIGH period of the SCL clock	32		-	ns
t_{DIG_L}	Logic LOW period of the SCL clock	32		-	ns
$t_{DIG\_H\_MIXED}$	Logic HIGH period of the SCL clock for mixed bus	32		-	ns
t_{HIGH_MIXED}	HIGH period of the SCL clock for mixed bus	24		-	ns
t_{SCO}	Clock in to data out for target			12	ns
t_{CR}	Fall time of SCL signal	-	$150/f_{SCL}$		ns
t_{CF}	Fall time of SCL signal	-	$150/f_{SCL}$		ns
t_{HD_PP}	SDA signal data hold in push-pull mode	0		-	ns
t_{SU_PP}	SDA signal data set up in push-pull mode	3		-	ns
t_{CASr}	Clock after repeated Start (Sr)	t_{CASmin}		-	ns
t_{CBSr}	Clock before repeated Start (Sr)	$t_{CASmin}/2$		-	ns
C_b	Capacitive load per bus line (SCL/SDA)	-		50	pF

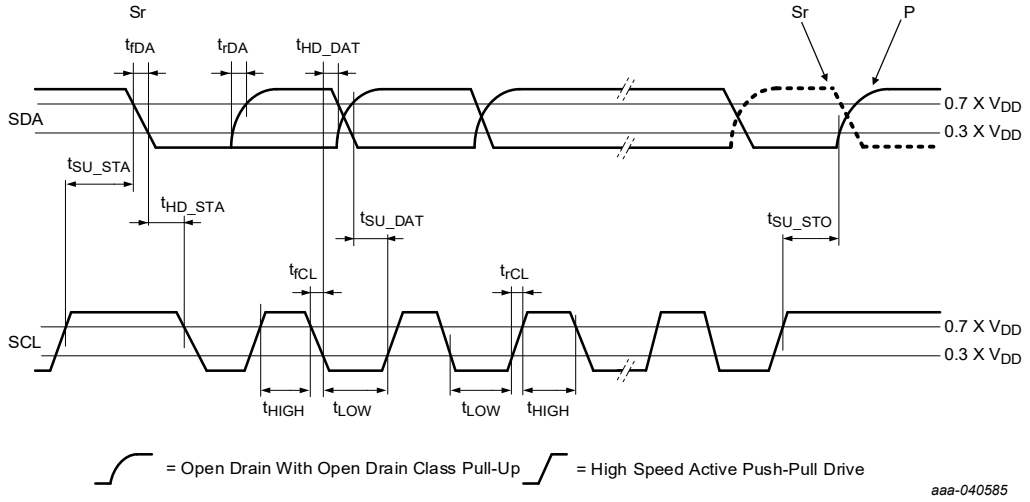
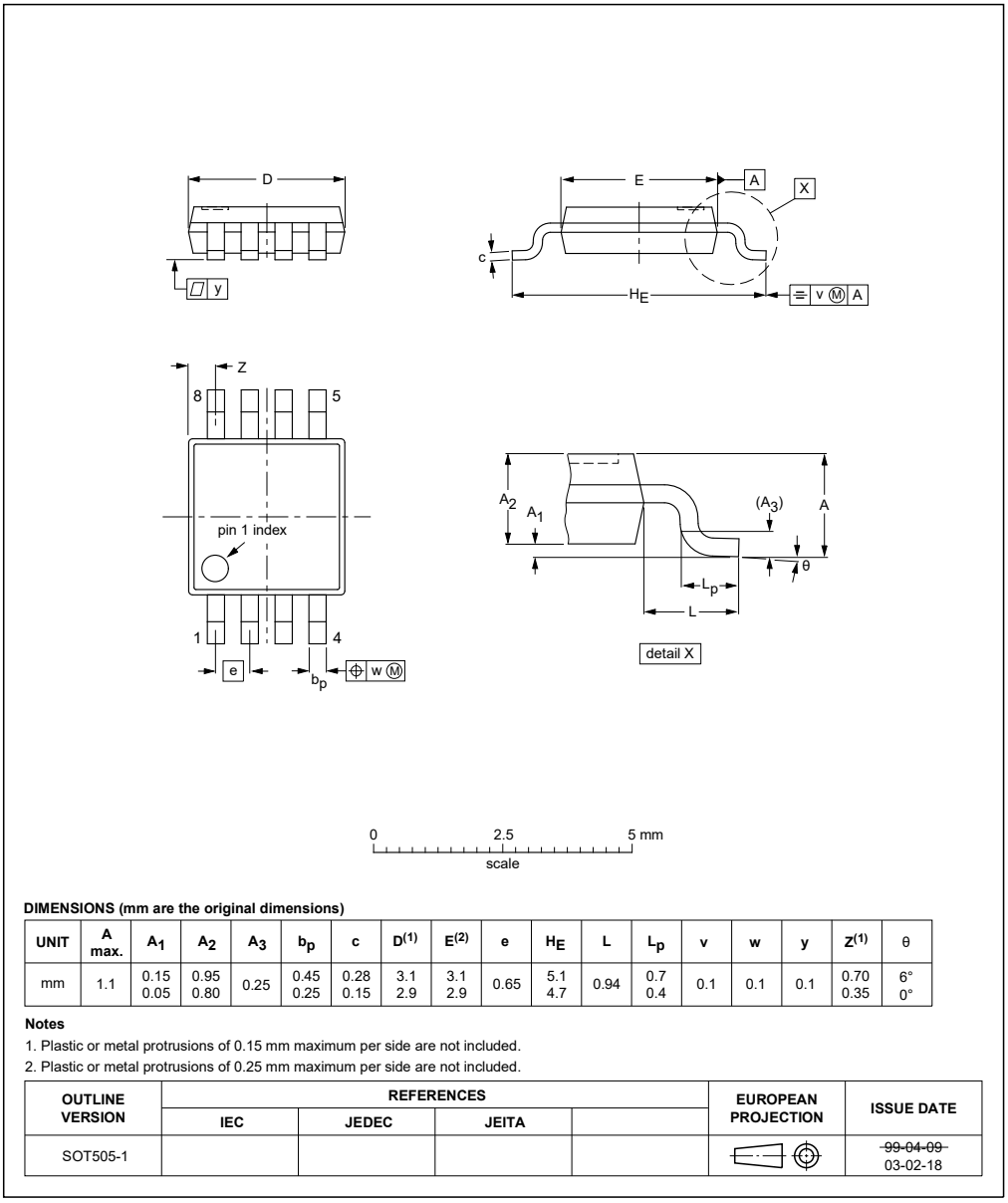


Figure 30. I3C timing diagram

13 Package outline

This section contains Figure 31, which illustrates the package outline for P3T1750DP.

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Figure 31. Package outline SOT505-1 (TSSOP8)

14 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 32) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 34 and Table 35

Table 34. SnPb eutectic process (from J-STD-020D)

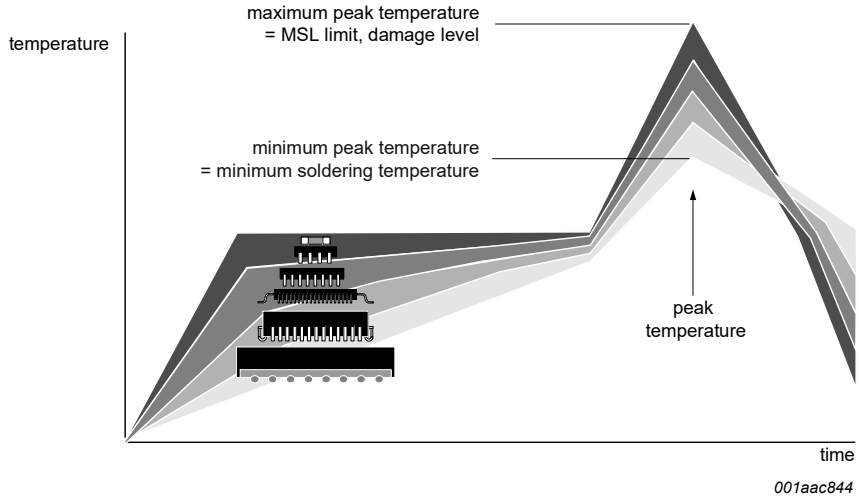
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 35. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 32.



MSL: Moisture Sensitivity Level

Figure 32. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15 Soldering: PCB footprints

This section provides PCB footprint figures for soldering the P3T1750DP.

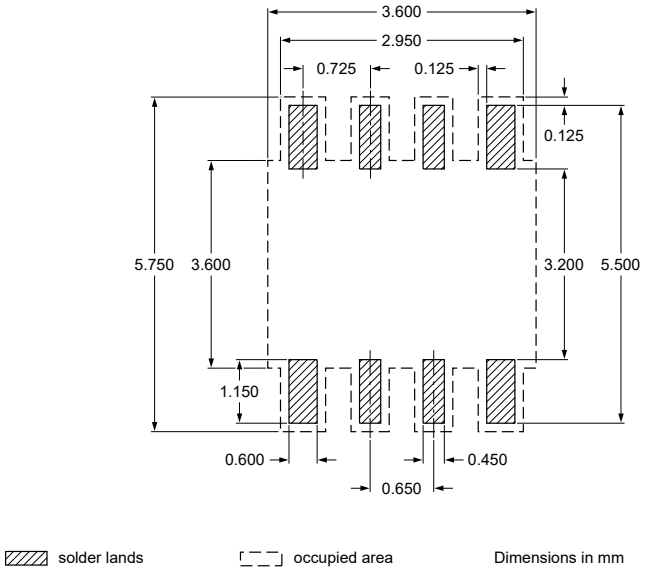


Figure 33. Reflow soldering footprint SOT505-1 (TSSOP8)

16 Acronyms

Table 36 describes the acronyms used in this data sheet.

Table 36. Acronyms

Acronym	Description
A-to-D	Analog-to-Digital
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
I2C-bus	Inter-Integrated Circuit Bus
I/O	Input/Output
LSB	Least Significant Bit
LSByte	Least Significant Byte
MSB	Most Significant Bit
MSByte	Most Significant Byte
PCB	Printed-Circuit Board
POR	Power-On Reset
SMD	Solder Mask Defined

17 Revision history

Table 37 summarizes revisions to this document.

Table 37. Revision history

Document ID	Release date	Description
P3T1750 v.1.2	8 October 2025	Updated per PCN #202510007F01: • Modified Table 30 • Editorial changes
P3T1750 v.1.1	15 July 2024	• Added Section 8.4 • Section 11: Updated conditions for V_{POR} • Section 7.4.5.1: Removed "..., or to signify a Hot-Join event (ENHJ/DISHJ)"
P3T1750 v.1.0	29 March 2023	• Initial public release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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