PCAL6524

Ultra Low-Voltage Translating 24-bit Fm+ I²C-bus/SMBus I/O Expander with Agile I/O Features, Interrupt Output, and Reset

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Document information

Information	Content
Keywords	PCAL6524, data sheet, remote I/O expansion, microcontroller
Abstract	The PCAL6524 is a 24-bit general-purpose I/O expander that provides remote I/O expansion for most microcontroller families via the fast-mode plus (Fm+) I^2C-bus interface.

1 General description

The PCAL6524 device is a 24-bit general-purpose I/O expander that provides remote I/O expansion for most microcontroller families via the fast-mode plus (Fm+) I^2C-bus interface. The ultra low-voltage interface allows for direct connection to a microcontroller operating down to 0.8 V.

NXP I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum. Some applications include battery-powered mobile applications for interfacing to sensors, push buttons, keypad, and so on. In addition to providing a flexible set of GPIOs, it simplifies interconnection of a processor running at one voltage level down to 0.8 V to I/O devices operating at a different voltage level 1.65 V to 5.5 V. The PCAL6524 has a built-in level shifting feature that makes these devices flexible in mixed power supply systems where communication between incompatible I/O voltages is required. This feature allows seamless communication with next-generation low-voltage microprocessors and microcontrollers on the interface side (SDA/SCL) and peripherals at higher voltage on the port side.

There are two supply voltages for PCAL6524: $V_{DD(I2C\text{-}bus)}$ and $V_{DD(P)}$. $V_{DD(I2C\text{-}bus)}$ provides the supply voltage for the interface at the controller side (for example, a microcontroller). $V_{DD(P)}$ provides the supply for core circuits and port P. The bidirectional voltage level translation in the PCAL6524 is provided through $V_{DD(I2C\text{-}bus)}$.

$V_{DD(I2C\text{-}bus)}$ must be connected to the V_{DD} of the external SCL/SDA lines. This operation indicates the V_{DD} level of the I^2C-bus to the PCAL6524, while $V_{DD(P)}$ determines the voltage level on port P of the PCAL6524.

The PCAL6524 fully meets the Fm+ I^2C-bus specification at speeds to 1 MHz and implements Agile I/O, which are additional features specifically designed to enhance the I/O. These additional features are: programmable output drive strength, latchable inputs, programmable pull-up/pull-down resistors, maskable interrupt, interrupt status register, and programmable open-drain or push-pull outputs.

Additional Agile I/O Plus features include I^2C software reset and device ID. Interrupts can be specified by level or edge, and can be cleared individually without disturbing the other interrupt events. Also, switch debounce hardware is implemented.

At power-on, the I/Os are configured as inputs. However, the system controller can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register, saving external logic gates. Programmable pull-up and pull-down resistors eliminate the need for discrete components.

The power-on reset puts the registers in their default state and initializes the I^2C-bus/SMBus state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without depowering the part. The system controller can also accomplish a reset via an I^2C command and initialize all registers to their default state.

The PCAL6524 open-drain interrupt ($\overline{\text{INT}}$) output is activated when any input state differs from its corresponding input port register state. As well, the $\overline{\text{INT}}$ output can be specified to activate on input pin edges. There are many interrupt mask functions available to maximize flexibility.

$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. Sending an interrupt signal on this line lets the remote I/O inform the microcontroller of any incoming data on its ports without communication via I^2C-bus. Therefore, the PCAL6524 can remain a simple target device. The input latch feature holds/latches the input pin state and keeps the logic values that created the interrupt until the controller can service the interrupt. This process minimizes the interrupt service response of the host for fast moving inputs.

The device port P outputs have 25 mA sink capabilities for directly driving LEDs while consuming low device current.

One hardware pin (ADDR) can be used to program and vary the fixed I^2C-bus address and allow up to four devices to share I^2C-bus or SMBus.

2 Features and benefits

- I^2C-bus to parallel port expander
- 1 MHz fast-mode plus I^2C-bus
- Operating power supply voltage range of 0.8 V to 3.6 V on the I^2C-bus side
- Allows bidirectional voltage-level translation and GPIO expansion between 0.8 V to 3.6 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V, 5.5 V port P
- Low standby current consumption: 2.0 μA typical at 3.3 V $V_{DD(P)}$
- Schmitt trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - V_{hys} = 0.05 V (typical) at 0.8 V
  - V_{hys} = 0.18 V (typical) at 1.8 V
  - V_{hys} = 0.33 V (typical) at 3.3 V
- 5.5 V tolerant I/O ports and 3.6 V tolerant I^2C-bus pins
- Active LOW reset input ($\overline{\text{RESET}}$)
- Open-drain active LOW interrupt output ($\overline{\text{INT}}$)
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 2000 V human-body model (A114-A)
  - 1000 V charged-device model (C101)
- Packages offered: HUQFN32, VFBGA36

2.1 Agile I/O features

- Output port configuration: bank selectable or pin selectable push-pull or open-drain output stages
- Interrupt status: read-only register identifies the source of an interrupt
- Bit-wise I/O programming features:
  - Output drive strength: four programmable drive strengths to reduce rise and fall times in low-capacitance applications
  - Input latch: Input port register values changes are kept until the input port register is read
  - Pull-up/pull-down enable: floating input or pull-up/pull-down resistor enable
  - Pull-up/pull-down selection: 100 kΩ pull-up/pull-down resistor selection
  - Interrupt mask: mask prevents the generation of the interrupt when input changes state to prevent spurious interrupts

2.2 Additional Agile I/O Plus features

- Interrupt edge specification on a bit-by-bit basis
- Interrupt individual clear without disturbing other events
- Read all interrupt events without clear
- Switch debounce hardware
- General call software reset
- I^2C software device ID function

3 Ordering information

Table 1 describes the ordering information for PCAL6524.

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCAL6524HE	L6524	HUQFN32	Plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.56 mm	SOT1426-1
PCAL6524EV	524	VFBGA36	Plastic very fine-pitch ball grid array package, body 2.6 x 2.6 mm	SOT1851-1

3.1 Ordering options

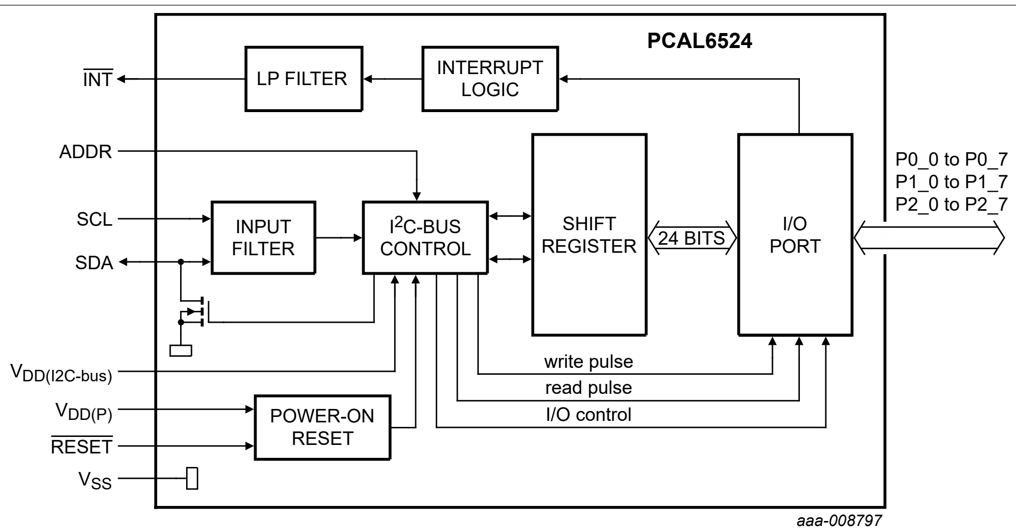
Table 2 describes the ordering options for PCAL6524.

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCAL6524HE	PCAL6524HEHP	HUQFN32	REEL 13" Q2/T3 * STA NDARD MARK SMD	5000	T_{amb} = -40 °C to +85 °C
	PCAL6524HEAZ	HUQFN32	REEL 7" Q2/T3 * STA NDARD MARK SMD	500	T_{amb} = -40 °C to +85 °C
PCAL6524EV	PCAL6524EVJ	VFBGA36	REEL 13" Q1/T1 *STANDARD MARK SMD	5000	T_{amb} = -40 °C to +85 °C

4 Block diagram

Figure 1 shows the labeled block diagram for PCAL6524.



All I/Os are set to inputs at reset.

Figure 1. Block diagram (positive logic)

5 Pinning information

This section provides the pin configuration and description of the VFBGA36 and HUQFN32 packages.

5.1 Pinning

Figure 2 and Figure 3 show the pinning for PCAL6524HE.

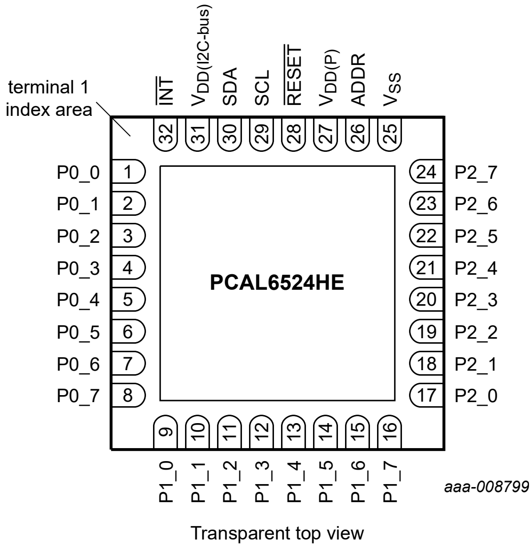


Figure 2. Pin configuration for HUQFN32

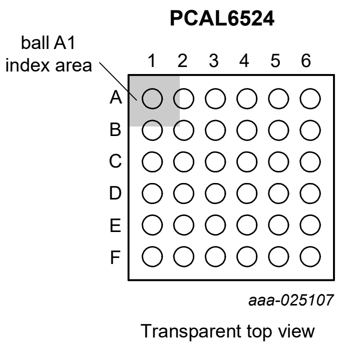


Figure 3. Pin configuration for VFBGA36

5.2 Pin description

Table 3 provides detailed description of various pins on PCAL6524.

Table 3. Pin description

Symbol	Pin		Type	Description
	VFBGA36	HUQFN32		
SCL	A3	29	I	Serial clock line. Connect to $V_{DD(I2C-bus)}$ through a pull-up resistor.
SDA	A2	30	I/O	Serial data line. Connect to $V_{DD(I2C-bus)}$ through a pull-up resistor.
$V_{DD(I2C-bus)}$	A1	31	Power supply	Supply voltage of the I²C-bus. Connect directly to the V_{DD} of the external I²C-bus controller. Provides voltage-level translation.

Table 3. Pin description...*continued*

Symbol	Pin		Type	Description
	VFBGA36	HUQFN32		
$\overline{\text{INT}}$	C4	32	O	Interrupt output. Connect to $V_{DD(I2C-bus)}$ or $V_{DD(P)}$ through a pull-up resistor.
P0_0[1]	B1	1	I/O	Port 0 input/output 0.
P0_1[1]	D4	2	I/O	Port 0 input/output 1.
P0_2[1]	C1	3	I/O	Port 0 input/output 2.
P0_3[1]	D2	4	I/O	Port 0 input/output 3.
P0_4[1]	D1	5	I/O	Port 0 input/output 4.
P0_5[1]	E1	6	I/O	Port 0 input/output 5.
P0_6[1]	D3	7	I/O	Port 0 input/output 6.
P0_7[1]	F1	8	I/O	Port 0 input/output 7.
P1_0[2]	E2	9	I/O	Port 1 input/output 0.
P1_1[2]	F2	10	I/O	Port 1 input/output 1.
P1_2[2]	E3	11	I/O	Port 1 input/output 2.
P1_3[2]	F3	12	I/O	Port 1 input/output 3.
P1_4[2]	F4	13	I/O	Port 1 input/output 4.
P1_5[2]	E4	14	I/O	Port 1 input/output 5.
P1_6[2]	F5	15	I/O	Port 1 input/output 6.
P1_7[2]	E5	16	I/O	Port 1 input/output 7.
P2_0[3]	F6	17	I/O	Port 2 input/output 0.
P2_1[3]	E6	18	I/O	Port 2 input/output 1.
P2_2[3]	D5	19	I/O	Port 2 input/output 2.
P2_3[3]	D6	20	I/O	Port 2 input/output 3.
P2_4[3]	C5	21	I/O	Port 2 input/output 4.
P2_5[3]	C6	22	I/O	Port 2 input/output 5.
P2_6[3]	B5	23	I/O	Port 2 input/output 6.
P2_7[3]	B6	24	I/O	Port 2 input/output 7.
V_{SS}	A6	25	Ground	Supply ground
ADDR	A5	26	I	Address input. Connect directly to $V_{DD(I2C-bus)}$, ground, SCL or SDA.
$V_{DD(P)}$	A4	27	Power supply	Supply voltage of PCAL6524 for Port P. 0.1 μF bypass capacitor required on this supply located as close to the package as practical.
$\overline{\text{RESET}}$	B4	28	I	Active LOW reset input. Connect to $V_{DD(I2C-bus)}$ through a pull-up resistor if no active connection is used.
n.c.	B2, B3, C2, C3	-	n.c.	Not connected

[1] Pins P0_0 to P0_7 correspond to bits P0.0 to P0.7. At power-on, all I/Os are configured as inputs.
[2] Pins P1_0 to P1_7 correspond to bits P1.0 to P1.7. At power-on, all I/Os are configured as inputs.
[3] Pins P2_0 to P2_7 correspond to bits P2.0 to P2.7. At power-on, all I/Os are configured as inputs.

6 Functional description

Refer to Figure 1.

6.1 Device address

Following a START condition, the bus controller must send the target address followed by a read ($R/\overline{W}$ = 1) or write ($R/\overline{W}$ = 0) operation bit. The target address of the PCAL6524 is shown in Figure 4. Target address pin ADDR chooses one of four target addresses. Table 4 shows all four target addresses by connecting the ADDR pin to SCL, SDA, V_{SS}, or V_{DD}.

Table 4. PCAL6524 address map

ADDR	Device family high-order address bits					Variable portion of address		Address
	A6	A5	A4	A3	A2	A1	A0	
SCL	0	1	0	0	0	0	0	40h
SDA	0	1	0	0	0	0	1	42h
V_{SS}	0	1	0	0	0	1	0	44h
V_{DD}	0	1	0	0	0	1	1	46h

The last bit of the first byte defines the reading from or writing to the PCAL6524. When set to logic 1 a read is selected, while logic 0 selects a write operation.

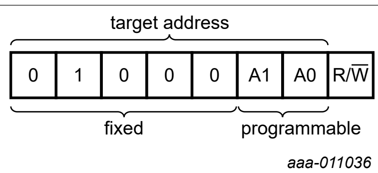


Figure 4. PCAL6524 address

6.2 Interface definition

Table 5 provides the interface definitions of PCAL6524.

Table 5. Interface definition

Byte	Bit							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I^2C-bus target address	L	H	L	L	L	A1	A0	$R/\overline{W}$
I/O data bus	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

6.3 Software reset call and device ID addresses

Two other different addresses can be sent to the device.

- General call address allows to reset the device through the I^2C-bus upon reception of the right I^2C-bus sequence. For details, see Section 6.3.1.

- Device ID address allows to read ID information from the device (manufacturer, part identification, revision). For details, see Section 6.3.2.

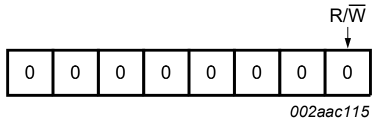


Figure 5. General call address

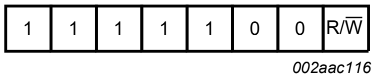


Figure 6. Device ID address

6.3.1 Software reset

The software reset call allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The software reset sequence is defined as follows:

1. The I²C-bus controller sends a START command.
2. The I²C-bus controller sends the reserved general call I²C-bus address '0000 000' with the R/W̄ bit set to 0 (write).
3. The device acknowledges after seeing the general call address '0000 0000' (00h) only. If the R/W̄ bit is set to 1 (read), no acknowledge is returned to the I²C-bus controller.
4. Once the general call address has been sent and acknowledged, the controller sends 1 byte. The value of the byte must be equal to 06h.
5. The device acknowledges this value only. If the byte is not equal to 06h, the device does not acknowledge it. If more than 1 byte of data is sent, the device does not acknowledge anymore.
6. Once the right byte has been sent and correctly acknowledged, the controller sends a STOP command to end the software reset sequence: the device then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the controller sends a Repeated START instead, no reset is performed.

The I²C-bus controller must interpret a non-acknowledge from the device (at any time) as a 'Software Reset Abort'. The device does not initiate a reset of its registers.

The unique sequence that initiates a software reset is described in Figure 7.

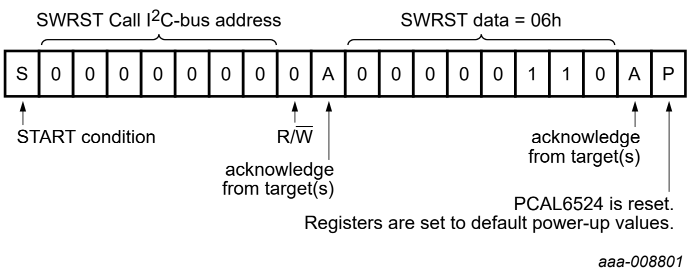


Figure 7. Software reset sequence

6.3.2 Device ID (PCAL6524 ID field)

The **Device ID** field is a 3-byte read-only (24 bits) word giving the following information:

- 12 bits with the manufacturer name, unique per manufacturer (for example, NXP).
- 9 bits with the part identification, assigned by manufacturer.
- 3 bits with the die revision, assigned by manufacturer (for example, Rev X).

The device ID is read-only, hardwired in the device and can be accessed as follows:

1. START command.
2. The controller sends the reserved device ID I²C-bus address followed by the R/$\overline{W}$ bit set to 0 (write): ‘1111 1000’.
3. The controller sends the I²C-bus target address of the target device it needs to identify. The LSB is a ‘Don’t care’ value. Only one device must acknowledge this byte (the one that has the I²C-bus target address).
4. The controller sends a Re-START command.
   Remark: A STOP command followed by a START command resets the target state machine and the device ID read cannot be performed. Also, a STOP command or a Re-START command followed by access to another target device resets the target state machine. In this case too, the device ID read cannot be performed.
5. The controller sends the reserved device ID I²C-bus address followed by the R/$\overline{W}$ bit set to 1 (read): ‘1111 1001’.
6. The device ID read can be done starting with the 12 manufacturer bits (first byte + 4 MSB of the second byte). It is followed by the 9 part identification bits (4 LSBs of the second byte + 5 MSBs of the third byte). It is further followed by the 3 die revision bits (3 LSBs of the third byte).
7. The controller ends the reading sequence by NACKing the last byte and thereby, resetting the target device state machine. This allows the controller to send the STOP command.
   Remark: The reading of the device ID can be stopped anytime by sending a NACK command.
   If the controller continues to ACK the bytes after the third byte, the target rolls back to the first byte. Now, the target keeps sending the device ID sequence until a NACK has been detected.
   For the PCAL6524, the device ID is as shown in Figure 8.

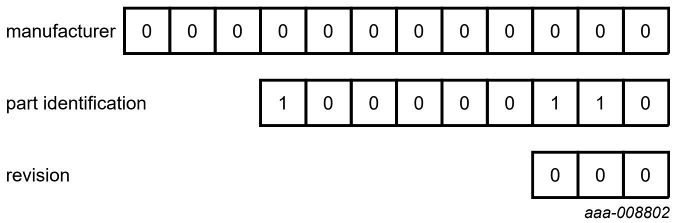
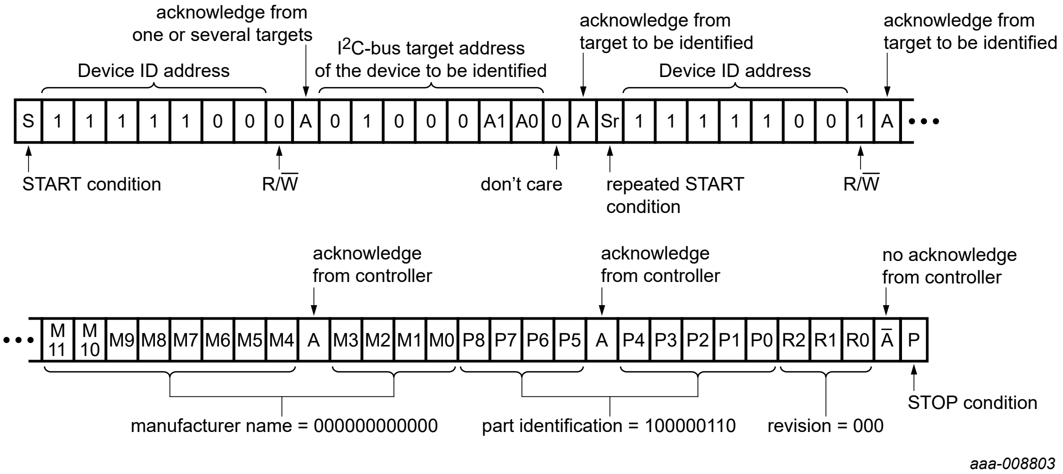


Figure 8. PCAL6524 device ID field



If more than 3 bytes are read, the target device loops back to the first byte (manufacturer byte). Now, the target device keeps sending data until the controller generates a 'no acknowledge'.

Figure 9. Device ID field reading

6.4 Pointer register and command byte

Following the successful acknowledgment of the target address byte, the bus controller sends a command byte, which is write only and stored in the pointer register in the PCAL6524. The lowest 7 bits (B[6:0] in Table 6) are used as a pointer to determine which register is accessed and the highest bit is used as Auto-Increment (AI) as shown in Figure 10. At power-up, hardware or software reset, the pointer register defaults to 00h, with AI bit set to '0' and the lowest seven bits set to '000 0000'.

When the AI bit is set (AI = 1), the seven low-order bits of the pointer register are automatically incremented after a read or write until a STOP condition is encountered. This process allows the user to program the registers sequentially without modifying the pointer register. The contents of these bits roll over to '000 0000' after the last register (address = 76h) is accessed. Unimplemented register addresses (reserved registers) are skipped. If more than 52 bytes are written, the address loops back to the register which is indicated by the seven low-order bits in the pointer register, and previously written data is overwritten. A STOP condition keeps the pointer register value in the last read or write location.

When the AI bit is cleared (AI = 0), the 2 least significant bits are automatically incremented after a read or write for the 3-register group which allows the user to program each of the 3-register group sequentially. If more than 3 bytes of data are read or written when AI is 0, previous data in the selected registers is overwritten. For example: if input port 1 is read first, the next 2nd byte will be input port 2, and the next 3rd byte will be input port 0. There is no limit on the number of data bytes for this read operation. There are two special 6-register groups: output drive strength (40h~45h) and interrupt edge (60h~65h) registers. These registers allow the user to program each of the 6-register group sequentially. Only the output port configuration register location (5Ch) remains in the same location after a successive read or write.

AI	B6	B5	B4	B3	B2	B1	B0	
0	0	0	0	0	0	0	0	default value at power-up or HW/SW reset

aaa-009085

AI = Auto-Increment

Figure 10. Pointer register bits

Table 6. Command byte

Pointer register bits							Command byte (hexadecimal)	Register	Protocol	Power-up default
B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	00h	Input port 0	Read byte	xxxx xxxx[1]
0	0	0	0	0	0	1	01h	Input port 1	Read byte	xxxx xxxx[1]
0	0	0	0	0	1	0	02h	Input port 2	Read byte	xxxx xxxx[1]
0	0	0	0	0	1	1	03h	Reserved[2]	Reserved	Reserved
0	0	0	0	1	0	0	04h	Output port 0	Read/write byte	1111 1111
0	0	0	0	1	0	1	05h	Output port 1	Read/write byte	1111 1111
0	0	0	0	1	1	0	06h	Output port 2	Read/write byte	1111 1111
0	0	0	0	1	1	1	07h	Reserved[2]	Reserved	Reserved
0	0	0	1	0	0	0	08h	Polarity Inversion port 0	Read/write byte	0000 0000
0	0	0	1	0	0	1	09h	Polarity Inversion port 1	Read/write byte	0000 0000
0	0	0	1	0	1	0	0Ah	Polarity Inversion port 2	Read/write byte	0000 0000
0	0	0	1	0	1	1	0Bh	Reserved[2]	Reserved	Reserved
0	0	0	1	1	0	0	0Ch	Configuration port 0	Read/write byte	1111 1111
0	0	0	1	1	0	1	0Dh	Configuration port 1	Read/write byte	1111 1111
0	0	0	1	1	1	0	0Eh	Configuration port 2	Read/write byte	1111 1111
-	-	-	-	-	-	-	0Fh to 3Fh	Reserved[2]	Reserved	Reserved
1	0	0	0	0	0	0	40h	Output drive strength register port 0A	Read/write byte	1111 1111
1	0	0	0	0	0	1	41h	Output drive strength register port 0B	Read/write byte	1111 1111
1	0	0	0	0	1	0	42h	Output drive strength register port 1A	Read/write byte	1111 1111
1	0	0	0	0	1	1	43h	Output drive strength register port 1B	Read/write byte	1111 1111
1	0	0	0	1	0	0	44h	Output drive strength register port 2A	Read/write byte	1111 1111
1	0	0	0	1	0	1	45h	Output drive strength register port 2B	Read/write byte	1111 1111
1	0	0	0	1	1	0	46h	Reserved[2]	Reserved	Reserved
1	0	0	0	1	1	1	47h	Reserved[2]	Reserved	Reserved
1	0	0	1	0	0	0	48h	Input latch register port 0	Read/write byte	0000 0000
1	0	0	1	0	0	1	49h	Input latch register port 1	Read/write byte	0000 0000
1	0	0	1	0	1	0	4Ah	Input latch register port 2	Read/write byte	0000 0000
1	0	0	1	0	1	1	4Bh	Reserved[2]	Reserved	Reserved
1	0	0	1	1	0	0	4Ch	Pull-up/pull-down enable register port 0	Read/write byte	0000 0000
1	0	0	1	1	0	1	4Dh	Pull-up/pull-down enable register port 1	Read/write byte	0000 0000
1	0	0	1	1	1	0	4Eh	Pull-up/pull-down enable register port 2	Read/write byte	0000 0000
1	0	0	1	1	1	1	4Fh	Reserved[2]	Reserved	Reserved

Table 6. Command byte...*continued*

Pointer register bits							Command byte (hexadecimal)	Register	Protocol	Power-up default
B6	B5	B4	B3	B2	B1	B0				
1	0	1	0	0	0	0	50h	Pull-up/pull-down selection register port 0	Read/write byte	1111 1111
1	0	1	0	0	0	1	51h	Pull-up/pull-down selection register port 1	Read/write byte	1111 1111
1	0	1	0	0	1	0	52h	Pull-up/pull-down selection register port 2	Read/write byte	1111 1111
1	0	1	0	0	1	1	53h	Reserved[2]	Reserved	Reserved
1	0	1	0	1	0	0	54h	Interrupt mask register port 0	Read/write byte	1111 1111
1	0	1	0	1	0	1	55h	Interrupt mask register port 1	Read/write byte	1111 1111
1	0	1	0	1	1	0	56h	Interrupt mask register port 2	Read/write byte	1111 1111
1	0	1	0	1	1	1	57h	Reserved[2]	Reserved	Reserved
1	0	1	1	0	0	0	58h	Interrupt status register port 0	Read byte	0000 0000
1	0	1	1	0	0	1	59h	Interrupt status register port 1	Read byte	0000 0000
1	0	1	1	0	1	0	5Ah	Interrupt status register port 2	Read byte	0000 0000
1	0	1	1	0	1	1	5Bh	Reserved[2]	Reserved	Reserved
1	0	1	1	1	0	0	5Ch[3]	Output port configuration register	Read/write byte	0000 0000
1	0	1	1	1	0	1	5Dh	Reserved[2]	Reserved	Reserved
1	0	1	1	1	1	0	5Eh	Reserved[2]	Reserved	Reserved
1	0	1	1	1	1	1	5Fh	Reserved[2]	Reserved	Reserved
1	1	0	0	0	0	0	60h	Interrupt edge register port 0A	Read/write byte	0000 0000
1	1	0	0	0	0	1	61h	Interrupt edge register port 0B	Read/write byte	0000 0000
1	1	0	0	0	1	0	62h	Interrupt edge register port 1A	Read/write byte	0000 0000
1	1	0	0	0	1	1	63h	Interrupt edge register port 1B	Read/write byte	0000 0000
1	1	0	0	1	0	0	64h	Interrupt edge register port 2A	Read/write byte	0000 0000
1	1	0	0	1	0	1	65h	Interrupt edge register port 2B	Read/write byte	0000 0000
1	1	0	0	1	1	0	66h	Reserved[2]	Reserved	Reserved
1	1	0	0	1	1	1	67h	Reserved[2]	Reserved	Reserved
1	1	0	1	0	0	0	68h	Interrupt clear register port 0	Write byte	0000 0000
1	1	0	1	0	0	1	69h	Interrupt clear register port 1	Write byte	0000 0000
1	1	0	1	0	1	0	6Ah	Interrupt clear register port 2	Write byte	0000 0000
1	1	0	1	0	1	1	6Bh	Reserved[2]	Reserved	Reserved
1	1	0	1	1	0	0	6Ch	Input status port 0	Read byte	xxxx xxxx[1]
1	1	0	1	1	0	1	6Dh	Input status port 1	Read byte	xxxx xxxx[1]
1	1	0	1	1	1	0	6Eh	Input status port 2	Read byte	xxxx xxxx[1]
1	1	0	1	1	1	1	6Fh	Reserved[2]	Reserved	Reserved

Table 6. Command byte...*continued*

Pointer register bits							Command byte (hexadecimal)	Register	Protocol	Power-up default
B6	B5	B4	B3	B2	B1	B0				
1	1	1	0	0	0	0	70h	Individual pin output port 0 configuration register	Read/write byte	0000 0000
1	1	1	0	0	0	1	71h	Individual pin output port 1 configuration register	Read/write byte	0000 0000
1	1	1	0	0	1	0	72h	Individual pin output port 2 configuration register	Read/write byte	0000 0000
1	1	1	0	0	1	1	73h	Reserved[2]	Reserved	Reserved
1	1	1	0	1	0	0	74h	Switch debounce enable 0	Read/write byte	0000 0000
1	1	1	0	1	0	1	75h	Switch debounce enable 1	Read/write byte	0000 0000
1	1	1	0	1	1	0	76h	Switch debounce count	Read/write byte	0000 0000
-	-	-	-	-	-	-	77h to 7Fh	Reserved[2]	Reserved	Reserved

[1] Undefined.
[2] These registers marked "reserved" should not be written, and the controller will not be acknowledged when accessed.
[3] Successive read and write accesses to remain at this register address.

6.5 Register descriptions

This section describes the PCAL6524 registers. It is further divided into the following subsections:

6.5.1 Input port registers (00h, 01h, 02h)

The input port registers (registers 00h, 01h, 02h) reflect the incoming logic levels of the pins. The input port registers are read only; writes to these registers have no effect and the transaction will be acknowledged (ACK). The default value ‘X’ is determined by the externally applied logic level. If a pin is configured as an output (registers 04h, 05h, 06h), the port value is equal to the actual voltage level on that pin. If the output is configured as open-drain (register 5Ch and registers 70h, 71h, 72h), the input port value is forced to 0. An input port register group read operation is performed as described in Section 7.2.

After reading input port registers, all interrupts are cleared.

Table 7. Input port 0 register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 8. Input port 1 register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

Table 9. Input port 2 register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	I2.7	I2.6	I2.5	I2.4	I2.3	I2.2	I2.1	I2.0
Default	X	X	X	X	X	X	X	X

6.5.2 Output port registers (04h, 05h, 06h)

The output port registers (registers 04h, 05h, 06h) show the outgoing logic levels of the pins defined as outputs by the configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, **not** the actual pin value. Section 7.1 describes a register group write and Section 7.2 describes a register group read.

Table 10. Output port 0 register (address 04h)

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 11. Output port 1 register (address 05h)

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

Table 12. Output port 2 register (address 06h)

Bit	7	6	5	4	3	2	1	0
Symbol	O2.7	O2.6	O2.5	O2.4	O2.3	O2.2	O2.1	O2.0
Default	1	1	1	1	1	1	1	1

6.5.3 Polarity inversion registers (08h, 09h, 0Ah)

The polarity inversion registers (registers 08h, 09h, 0Ah) allow polarity inversion of pins defined as inputs by the configuration register. If a bit in these registers is set (written with ‘1’), the corresponding port pin’s polarity is inverted in the input register. If a bit in this register is cleared (written with a ‘0’), the corresponding port pin’s polarity is retained. Section 7.1 describes a register group write and Section 7.2 describes a register group read.

Table 13. Polarity inversion port 0 register (address 08h)

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 14. Polarity inversion port 1 register (address 09h)

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0

Table 14. Polarity inversion port 1 register (address 09h)*...continued*

Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0

Table 15. Polarity inversion port 2 register (address 0Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	N2.7	N2.6	N2.5	N2.4	N2.3	N2.2	N2.1	N2.0
Default	0	0	0	0	0	0	0	0

6.5.4 Configuration registers (0Ch, 0Dh, 0Eh)

The configuration registers (registers 0Ch, 0Dh, 0Eh) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output. Section 7.1 describes a register group write and Section 7.2 describes a register group read.

Table 16. Configuration port 0 register (address 0Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 17. Configuration port 1 register (address 0Dh)

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

Table 18. Configuration port 2 register (address 0Eh)

Bit	7	6	5	4	3	2	1	0
Symbol	C2.7	C2.6	C2.5	C2.4	C2.3	C2.2	C2.1	C2.0
Default	1	1	1	1	1	1	1	1

6.5.5 Output drive strength registers (40h, 41h, 42h, 43h, 44h, 45h)

The output drive strength registers control the output drive level of the GPIO. Each GPIO can be configured independently to a certain output current level by two register control bits. For example, register 41h CC0.7 (bits [7:6]) controls port 0.7 and register 41h CC0.6 (bits [5:4]) controls port 0.6. The output drive level of the GPIO is programmed: 00b = 0.25×, 01b = 0.5×, 10b = 0.75× or 11b = 1× of the drive capability of the I/O. For details, see Section 8.1. Section 7.1 describes a register group write and Section 7.2 describes a register group read.

Table 19. Current control port 0A register (address 40h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.3		CC0.2		CC0.1		CC0.0	
Default	1	1	1	1	1	1	1	1

Table 20. Current control port 0B register (address 41h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.7		CC0.6		CC0.5		CC0.4	
Default	1	1	1	1	1	1	1	1

Table 21. Current control port 1A register (address 42h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.3		CC1.2		CC1.1		CC1.0	
Default	1	1	1	1	1	1	1	1

Table 22. Current control port 1B register (address 43h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.7		CC1.6		CC1.5		CC1.4	
Default	1	1	1	1	1	1	1	1

Table 23. Current control port 2A register (address 44h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC2.3		CC2.2		CC2.1		CC2.0	
Default	1	1	1	1	1	1	1	1

Table 24. Current control port 2B register (address 45h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC2.7		CC2.6		CC2.5		CC2.4	
Default	1	1	1	1	1	1	1	1

6.5.6 Input latch registers (48h, 49h, 4Ah)

The input latch registers (registers 48h, 49h, 4Ah) enable and disable the input latch of the I/O pins. These registers are effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change in the corresponding input pin generates an interrupt. A read of the input register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared.

When an input latch register bit is 1, the corresponding input pin state is latched. A change of state of the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (registers 0, 1 and 2). A read of the input port register clears the interrupt. If the input pin returns to its initial logic state before the input port register is read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt. See Figure 20.

For example, if the P0_4 input was as logic 0 and the input goes to logic 1 then back to logic 0, the input port 0 register captures this change and an interrupt is generated (if unmasked). When the read is performed on the input port 0 register, the interrupt is cleared, assuming there were no additional inputs that have changed, and bit 4 of the input port 0 register reads ‘1’. The next read of the input port register bit 4 register should now read ‘0’.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input register reflects only the change of state of the latched input and also clears the interrupt. The interrupt is cleared if the input latch register changes from latched to non-latched configuration and the I/O pin returns to its original state.

If the input pin is changed from latched to non-latched input, a read from the input port register reflects the current port logic level. If the input pin is changed from non-latched to latched input, the read from the input register reflects the latched logic level. Section 7.1 describes a register group write and Section 7.2 describes a register group read.

Table 25. Input latch port 0 register (address 48h)

Bit	7	6	5	4	3	2	1	0
Symbol	L0.7	L0.6	L0.5	L0.4	L0.3	L0.2	L0.1	L0.0
Default	0	0	0	0	0	0	0	0

Table 26. Input latch port 1 register (address 49h)

Bit	7	6	5	4	3	2	1	0
Symbol	L1.7	L1.6	L1.5	L1.4	L1.3	L1.2	L1.1	L1.0
Default	0	0	0	0	0	0	0	0

Table 27. Input latch port 2 register (address 4Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	L2.7	L2.6	L2.5	L2.4	L2.3	L2.2	L2.1	L2.0
Default	0	0	0	0	0	0	0	0

6.5.7 Pull-up/pull-down enable registers (4Ch, 4Dh, 4Eh)

The pull-up and pull-down enable registers allow the user to enable or disable pull-up/pull-down resistors on the I/O pins. Setting the bit to logic 1 enables the selection of pull-up/pull-down resistors. Setting the bit to logic 0 disconnects the pull-up/pull-down resistors from the I/O pins. Also, the resistors will be disconnected when the outputs are configured as open-drain outputs (see Section 6.5.11 and Section 6.5.15). Use the pull-up/pull-down registers to select either a pull-up or pull-down resistor. Section 7.1 describes a register group write and Section 7.2 describes a register group read.

Table 28. Pull-up/pull-down enable port 0 register (address 4Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	PE0.7	PE0.6	PE0.5	PE0.4	PE0.3	PE0.2	PE0.1	PE0.0
Default	0	0	0	0	0	0	0	0

Table 29. Pull-up/pull-down enable port 1 register (address 4Dh)

Bit	7	6	5	4	3	2	1	0
Symbol	PE1.7	PE1.6	PE1.5	PE1.4	PE1.3	PE1.2	PE1.1	PE1.0

Table 29. Pull-up/pull-down enable port 1 register (address 4Dh)*...continued*

Bit	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0

Table 30. Pull-up/pull-down enable port 2 register (address 4Eh)

Bit	7	6	5	4	3	2	1	0
Symbol	PE2.7	PE2.6	PE2.5	PE2.4	PE2.3	PE2.2	PE2.1	PE2.0
Default	0	0	0	0	0	0	0	0

6.5.8 Pull-up/pull-down selection registers (50h, 51h, 52h)

The I/O port can be configured to have a pull-up or pull-down resistor by programming the pull-up/pull-down selection register. Setting a bit to logic 1 selects a 100 kΩ pull-up resistor for that I/O pin. Setting a bit to logic 0 selects a 100 kΩ pull-down resistor for that I/O pin. If the pull-up/down feature is disconnected, writing to this register has no effect on the I/O pin. The typical value is 100 kΩ with a minimum of 50 kΩ and a maximum of 150 kΩ. Section 7.1 describes a register group write operation and Section 7.2 describes a register group read operation.

Table 31. Pull-up/pull-down selection port 0 register (address 50h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD0.7	PUD0.6	PUD0.5	PUD0.4	PUD0.3	PUD0.2	PUD0.1	PUD0.0
Default	1	1	1	1	1	1	1	1

Table 32. Pull-up/pull-down selection port 1 register (address 51h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD1.7	PUD1.6	PUD1.5	PUD1.4	PUD1.3	PUD1.2	PUD1.1	PUD1.0
Default	1	1	1	1	1	1	1	1

Table 33. Pull-up/pull-down selection port 2 register (address 52h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD2.7	PUD2.6	PUD2.5	PUD2.4	PUD2.3	PUD2.2	PUD2.1	PUD2.0
Default	1	1	1	1	1	1	1	1

6.5.9 Interrupt mask registers (54h, 55h, 56h)

Interrupt mask registers are set to logic 1 upon power-on, disabling interrupts during system start-up. Interrupts can be enabled by setting the corresponding mask bits to logic 0.

If an input changes state and the corresponding bit in the interrupt mask register is set to 1, the interrupt is masked and the interrupt pin will not be asserted. If the corresponding bit in the Interrupt mask register is set to 0, the interrupt pin is asserted.

When an input changes state and the resulting interrupt is masked (interrupt mask bit is 1), setting the input mask register bit to 0 will cause the interrupt pin to be asserted. If the interrupt mask bit of an input that is the source of an interrupt is set to 1, the interrupt pin is de-asserted. Section 7.1 describes a register group write operation and Section 7.2 describes a register group read operation.

Table 34. Interrupt mask port 0 register (address 54h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M0.7	M0.6	M0.5	M0.4	M0.3	M0.2	M0.1	M0.0
Default	1	1	1	1	1	1	1	1

Table 35. Interrupt mask port 1 register (address 55h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M1.7	M1.6	M1.5	M1.4	M1.3	M1.2	M1.1	M1.0
Default	1	1	1	1	1	1	1	1

Table 36. Interrupt mask port 2 register (address 56h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M2.7	M2.6	M2.5	M2.4	M2.3	M2.2	M2.1	M2.0
Default	1	1	1	1	1	1	1	1

6.5.10 Interrupt status registers (58h, 59h, 5Ah)

The read-only interrupt status registers are used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt.

When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit will return logic 0. Section 7.2 describes a register group read operation.

Table 37. Interrupt status port 0 register (address 58h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S0.7	S0.6	S0.5	S0.4	S0.3	S0.2	S0.1	S0.0
Default	0	0	0	0	0	0	0	0

Table 38. Interrupt status port 1 register (address 59h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S1.7	S1.6	S1.5	S1.4	S1.3	S1.2	S1.1	S1.0
Default	0	0	0	0	0	0	0	0

Table 39. Interrupt status port 2 register (address 5Ah) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S2.7	S2.6	S2.5	S2.4	S2.3	S2.2	S2.1	S2.0
Default	0	0	0	0	0	0	0	0

6.5.11 Output port configuration register (5Ch)

The output port configuration register selects a port-wise push-pull or open-drain I/O stage. A logic 0 configures the I/O as push-pull (Q1 and Q2 are active, see Figure 11). A logic 1 configures the I/O as open-drain (Q1 is disabled, Q2 is active) and the recommended command sequence is to program this register (5Ch) before the configuration register (0Ch, 0Dh, 0Eh) sets the port pins as outputs.

ODEN0 configures port 0_x, ODEN1 configures port 1_x, and ODEN2 configures port 2_x.

Individual pins may be programmed as open-drain or push-pull by programming individual pin output configuration registers (70h, 71h, 72h). For details, see Section 6.5.15.

A register group read or write operation is not allowed on this register. Successive read or write accesses remain at this register address.

Table 40. Output port configuration register (address 5Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	Reserved					ODEN2	ODEN1	ODEN0
Default	0	0	0	0	0	0	0	0

6.5.12 Interrupt edge registers (60h, 61h, 62h and 63h, 64h, 65h)

The interrupt edge registers determine what action on an input pin causes an interrupt along with the interrupt mask registers (54h, 55h, and 56h). If the Interrupt is enabled (set ‘0’ in the mask register) and the action at the corresponding pin matches the required activity, the $\overline{\text{INT}}$ output becomes active. The default value for each pin is 00b or level triggered, meaning a level change on the pin will cause an interrupt event. A level triggered action means a change in logic state (HIGH-to-LOW or LOW-to-HIGH), since the last read of the Input port (00h, 01h, or 02h) which can be latched with a corresponding ‘1’ set in the input latch register (48h, 49h, 4Ah). If the Interrupt edge register entry is set to 11b, any edge, positive or negative going, causes an interrupt event. If an entry is 01b, only a positive-going edge causes an interrupt event, while a 10b requires a negative-going edge to cause an interrupt event. These edge interrupt events are latched, regardless of the status of the input latch register (48h, 49h, 4Ah). These edged interrupts can be cleared in several ways: reading input port registers (00h, 01h, 02h); setting the interrupt mask register (54h, 55h, 56h) to 1 (masked); setting the interrupt clear register (68h, 69h, 6Ah) to 1 (this is a write-only register); resetting the interrupt edge register (60h to 65h) back to 0. Section 7.1 describes a register group write operation and Section 7.2 describes a register group read operation.

Table 41. Interrupt edge port 0A register (address 60h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE0.3		IE0.2		IE0.1		IE0.0	
Default	0	0	0	0	0	0	0	0

Table 42. Interrupt edge port 0B register (address 61h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE0.7		IE0.6		IE0.5		IE0.4	
Default	0	0	0	0	0	0	0	0

Table 43. Interrupt edge port 1A register (address 62h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE1.3		IE1.2		IE1.1		IE1.0	
Default	0	0	0	0	0	0	0	0

Table 44. Interrupt edge port 1B register (address 63h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE1.7		IE1.6		IE1.5		IE1.4	
Default	0	0	0	0	0	0	0	0

Table 45. Interrupt edge port 2A register (address 64h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE2.3		IE2.2		IE2.1		IE2.0	
Default	0	0	0	0	0	0	0	0

Table 46. Interrupt edge port 2B register (address 65h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE2.7		IE2.6		IE2.5		IE2.4	
Default	0	0	0	0	0	0	0	0

Table 47. Interrupt edge bits (IEx.x)

Bit 1	Bit 0	Description
0	0	Level-triggered interrupt
0	1	Positive-going (rising) edge triggered interrupt
1	0	Negative-going (falling) edge triggered interrupt
1	1	Any edge (positive or negative-going) triggered interrupt

6.5.13 Interrupt clear registers (68h, 69h, 6Ah)

The write-only interrupt clear registers clear individual interrupt sources (status bit). Setting an individual bit or any combination of bits to logic 1 will reset the corresponding interrupt source, so if that source was the only event causing an interrupt, the $\overline{\text{INT}}$ will be cleared. After writing a logic 1, the bit returns to logic 0. Section 7.1 describes a register group write operation.

Table 48. Interrupt clear port 0 register (address 68h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IC0.7	IC0.6	IC0.5	IC0.4	IC0.3	IC0.2	IC0.1	IC0.0
Default	0	0	0	0	0	0	0	0

Table 49. Interrupt clear port 1 register (address 69h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IC1.7	IC1.6	IC1.5	IC1.4	IC1.3	IC1.2	IC1.1	IC1.0
Default	0	0	0	0	0	0	0	0

Table 50. Interrupt clear port 2 register (address 6Ah) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IC2.7	IC2.6	IC2.5	IC2.4	IC2.3	IC2.2	IC2.1	IC2.0
Default	0	0	0	0	0	0	0	0

6.5.14 Input status registers (6Ch, 6Dh, 6Eh)

The read-only input status registers function exactly like input port 0, 1 and 2 (00h, 01h, 02h) without resetting the interrupt logic. This allows inspection of the actual state of the input pins without upsetting internal logic. If the pin is configured as an input, the port read is unaffected by input latch logic or other features, the state of the register is simply a reflection of the current state of the input pins. If a pin is configured as an output by the configuration register (0Ch, 0Dh, 0Eh), and is also configured as open-drain (register 5Ch and 70h, 71h, 72h), the read for that pin will always return 0, otherwise that state of that pin is returned. Section 7.2 descibes a register group read operation.

Table 51. Input status port 0 register (address 6Ch) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	II0.7	II0.6	II0.5	II0.4	II0.3	II0.2	II0.1	II0.0
Default	X	X	X	X	X	X	X	X

Table 52. Input status port 1 register (address 6Dh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	II1.7	II1.6	II1.5	II1.4	II1.3	II1.2	II1.1	II1.0
Default	X	X	X	X	X	X	X	X

Table 53. Input status port 2 register (address 6Eh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	II2.7	II2.6	II2.5	II2.4	II2.3	II2.2	II2.1	II2.0
Default	X	X	X	X	X	X	X	X

6.5.15 Individual pin output configuration registers (70h, 71h, 72h)

The individual pin output configuration registers modify the output configuration (push-pull or open-drain) set by the output port configuration register (5Ch).

If the ODENx bit is set at logic 0 (push-pull), any bit set to logic 1 in the IOCRx register reverses the output state of that pin only to open-drain. When the ODENx bit is set at logic 1 (open-drain), a logic 1 in IOCRx sets that pin to push-pull.

The recommended command sequence to program the output pin is to program ODENx (5Ch), the IOCRx, and finally the configuration register (0Ch, 0Dh, 0Eh) to set the pins as outputs. Section 7.1 describes a register group write operation and Section 7.2 describes a register group read operation.

Table 54. Individual pin output configuration register 0 (address 70h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR0.7	IOCR0.6	IOCR0.5	IOCR0.4	IOCR0.3	IOCR0.2	IOCR0.1	IOCR0.0
Default	0	0	0	0	0	0	0	0

Table 55. Individual pin output configuration register 1 (address 71h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR1.7	IOCR1.6	IOCR1.5	IOCR1.4	IOCR1.3	IOCR1.2	IOCR1.1	IOCR1.0
Default	0	0	0	0	0	0	0	0

Table 56. Individual pin output configuration register 2 (address 72h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR2.7	IOCR2.6	IOCR2.5	IOCR2.4	IOCR2.3	IOCR2.2	IOCR2.1	IOCR2.0
Default	0	0	0	0	0	0	0	0

6.5.16 Switch debounce enable registers (74h, 75h)

The switch debounce enable registers enable the switch debounce function for port 0 and port 1 pins. If a pin on port 0 or port 1 is designated as an input, a logic 1 in the switch debounce enable register connects the debounce logic to that pin. If a pin is assigned as an output (via configuration port 0 or port 1 register), the debounce logic is not connected to that pin, and it functions as a normal output. The switch debounce logic requires an oscillator time base input and if this function is used, P0_0 is designated as the oscillator input. If P0_0 is not configured as input and if SD0.0 is not set to logic 1, the switch debounce logic is not connected to any pin. For details on switch debounce logic functionality, see Section 6.10.

Table 57. Switch debounce enable port 0 register (address 74h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	SD0.7	SD0.6	SD0.5	SD0.4	SD0.3	SD0.2	SD0.1	SD0.0
Default	0	0	0	0	0	0	0	0

Table 58. Switch debounce enable port 1 register (address 75h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	SD1.7	SD1.6	SD1.5	SD1.4	SD1.3	SD1.2	SD1.1	SD1.0
Default	0	0	0	0	0	0	0	0

6.5.17 Switch debounce count register (76h)

The switch debounce count register is used to count the debounce time that the switch debounce logic uses to determine if a switch connected to one of the port 0 or port 1 pins finally stays open (logic 1) or closed (logic

0). This number, together with the oscillator frequency supplied to P0_0, determines the debounce time (for example, the debounce time will be 10 μs if this register is set to 0Ah and external oscillator frequency is 1 MHz). For details, see Section 6.10.

Table 59. Switch debounce count register (address 76h) bit description [1]

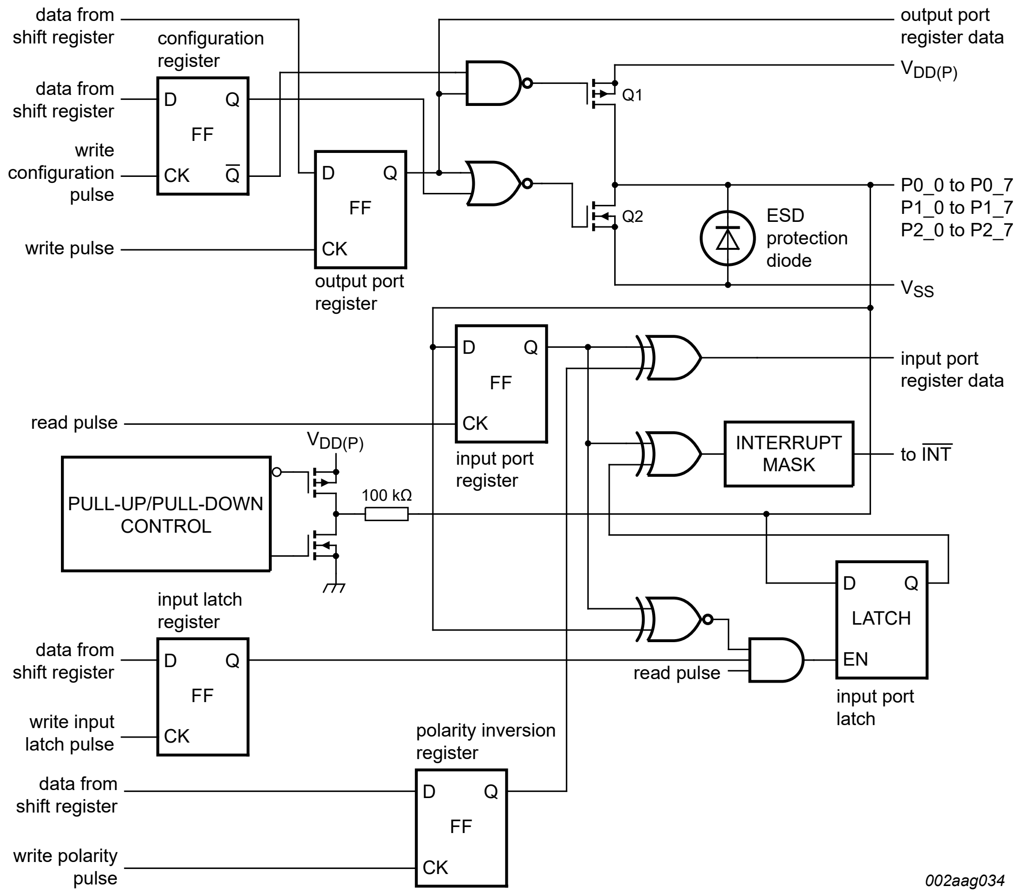
Bit	7	6	5	4	3	2	1	0
Symbol	SDC0.7	SDC0.6	SDC0.5	SDC0.4	SDC0.3	SDC0.2	SDC0.1	SDC0.0
Default	0	0	0	0	0	0	0	0

[1] The switch debounce logic is disabled if this register is set to 00h.

6.6 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above $V_{DD(P)}$ to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either $V_{DD(P)}$ or V_{SS}. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation. To avoid internal noise generation when multiple outputs switch simultaneously, a 0.1 μF bypass capacitor is required on the $V_{DD(P)}$ pin as close to the package as practical.



On power-up or reset, all registers return to default values.

Figure 11. Simplified schematic of P0_0 to P2_7

6.7 Power-on reset

When power (from 0 V) is applied to $V_{DD(P)}$, an internal power-on reset holds the PCAL6524 in a reset condition until $V_{DD(P)}$ has reached V_{POR}. At that time, the reset condition is released and the PCAL6524 registers and I^2C-bus/SMBus state machine initializes to their default states. After that, $V_{DD(P)}$ must be lowered to below V_{POR} and back up to the operating voltage for a power-reset cycle. For details, see Section 8.2.

6.8 Reset input (RESET)

The $\overline{\text{RESET}}$ input can be asserted to initialize the system while keeping the $V_{DD(P)}$ at its operating level. A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of $t_{w(rst)}$. The PCAL6524 registers and I^2C-bus/SMBus state machine are changed to their default state once $\overline{\text{RESET}}$ is LOW (0). When $\overline{\text{RESET}}$ is HIGH (1), the I/O levels at the P port can be changed externally or through the controller. This input requires a pull-up resistor to $V_{DD(I2C\text{-}bus)}$ if no active connection is used.

6.9 Interrupt output (INT)

The $\overline{\text{INT}}$ output has an open-drain structure and requires a pull-up resistor to $V_{DD(P)}$ or $V_{DD(I2C\text{-}bus)}$ depending on the application. When any current input port state differs from its corresponding input port register state, the interrupt output pin is asserted (logic 0) to indicate the system controller (MCU) that one of the input port states has changed. A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input can cause a false interrupt to occur if the state of the pin does not match the contents of the input port register.

To enable the interrupt output, the following three conditions must be satisfied:

- The GPIO must be configured as an input port by writing "1" to configuration port registers (0Ch, 0Dh, 0Eh)
- The interrupt mask registers (54h, 55h, 56h) must be set to "0" to unmask interrupt sources.
- The interrupt edge registers (60h to 65h) select what action on each input pin causes an interrupt; there are four different interrupt trigger modes: level trigger, rising-edge trigger, falling-edge trigger, or any edge trigger.

The input latch registers (48h, 49h, 4Ah) control each input pin either to enable latched input state or non-latched input state. When the input pin is set to latch state, it will hold or latch the input pin state (keep the logic value) and generate an interrupt until the controller can service the interrupt. This minimizes the host's interrupt service response for fast moving inputs.

Any interrupt status bit can be cleared and $\overline{\text{INT}}$ pin de-asserted by using one of the following methods and conditions:

- Power-on reset (POR), hardware reset from $\overline{\text{RESET}}$ pin, or software reset call
- Read input port registers (00h, 01h, 02h)
- Write logic 1 to interrupt clear registers (68h, 69h, 6Ah)
- Write logic 1 to interrupt mask registers (54h, 55h, 56h)
- Write logic 0 to configuration registers (0Ch, 0Dh, 0Eh), set pin as output port.
- Input pin goes back to its initial state in level trigger and non-latch mode
- Input pin goes back to its initial state in level trigger. Change latch to non-latch mode
- Change the interrupt trigger mode from level trigger to edge trigger or vice versa in interrupt edge registers

When using the input latch feature, the input pin state is latched. The interrupt is de-asserted only when data is read from the port that generated the interrupt. The interrupt reset occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be short) due to the resetting of the interrupt during this pulse. Any change of the inputs after resetting is detected and is transmitted as $\overline{\text{INT}}$.

6.10 Switch debounce circuitry

Mechanical switches do not make clean make-or-break connections. The contacts can 'bounce' for a significant period before settling into a steady-state condition. This situation can confuse fast processors and make the physical interface difficult to design and the software interface difficult to make reliable.

The PCAL6524 implements hardware to ease the hardware interface by debouncing switch closures with dedicated circuitry. P0_1 to P0_7, P1_0 to P1_7 can connect to this debounce hardware on a pin-by-pin basis. These switch debouncers remove bounce when a switch opens or closes by requiring that sequentially clocked inputs remain in the same state for several sampling periods. The output does not change until the input is stable for a programmable duration. The circuit block diagram (Figure 13) shows the functional blocks consisting of an external oscillator, counter, edge detector, and D flip-flop. When the switch input state changes, the edge detector resets the counter. When the switch input state is stable for the full qualification period, the counter clocks the flip-flop, updating the output. Figure 14 shows the typical opening and closing switch debounce operation timing.

To use the debounce circuitry, set the port pins (P0_1 to P0_7, and P1_0 to P1_7) with switches attached in the switch debounce enable 0 and 1 registers (74h, 75h). Connect an external oscillator signal on P0_0, which serves as a time base to the debounce timer. Finally, set a delay time in the switch debounce count register (76h). The combination of the time base of the external oscillator and the debounce count sets the qualification debounce period or t_{DP} in Figure 14. All debounce counters use the same time base and count, but they all function independently.

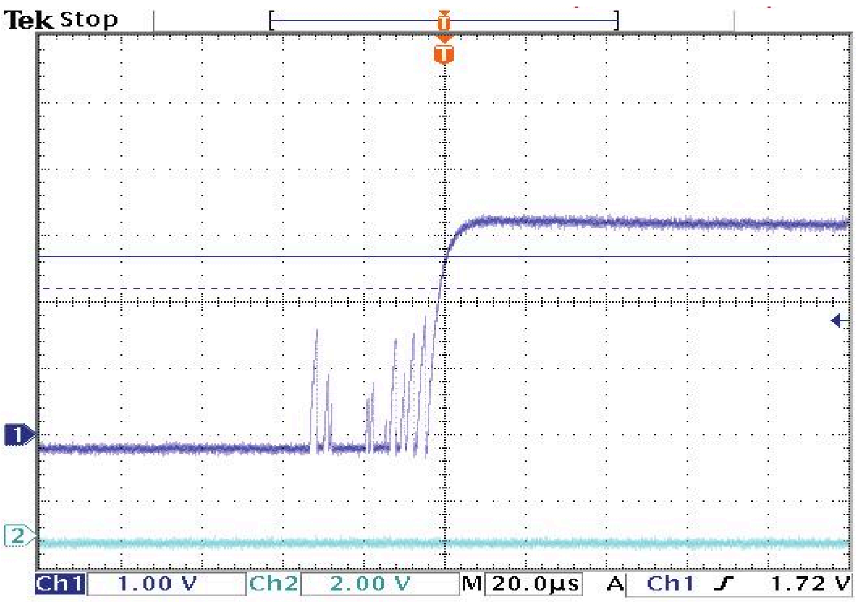
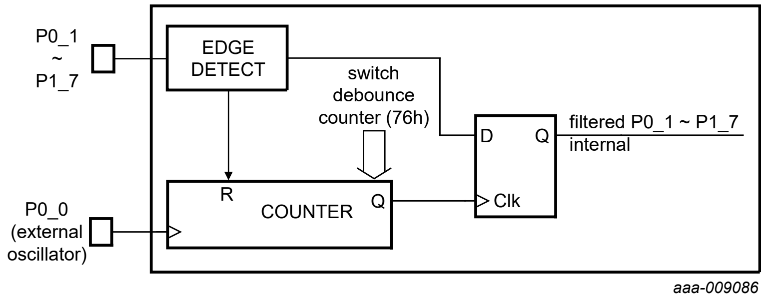
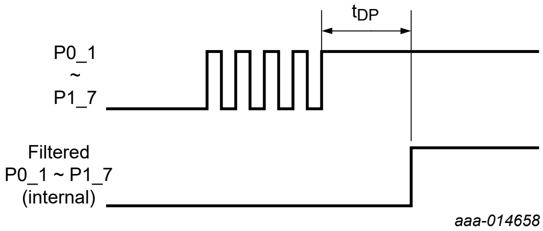


Figure 12. Switch contact bounce



When the external clock connects for the first time, it is required to wait 9 clock cycles for the debounce circuit in normal operation.

Figure 13. Debouncer block diagram



t_{DP} = [PERIOD of EXT CLOCK] * [Debounce counter(76h)] = 1 μs * 10 = 10 μs (if external clock = 1 MHz, debounce count register (76h) = 0Ah)

Figure 14. Switch debounce timing

7 Bus transactions

PCAL6524 is an I^2C-bus target device. Data is exchanged between the controller and PCAL6524 through write and read commands using I^2C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Write commands

Data is transmitted to PCAL6524 by sending the device address with the least significant bit (LSB) set to a logic 0 (for details on device address, see Figure 4). The command byte is sent after the address and determines which register receives the data that follows the command byte.

Many of the registers within the PCAL6524 are configured to operate as register triples. The groups are input ports, output ports, polarity inversion and configuration registers, as well as input latch, pull-up/pull-down enable and selection registers, interrupt mask and interrupt status, interrupt clear and input port (status) without interrupt clear registers, individual pin output port configuration registers, and switch debounce registers. After sending data to one register, the next data byte is sent to the next register in the group. For example, if the first byte is sent to output port 1 (register 05h), the next byte is stored in output port 2 (register 06h). The next byte sent is stored in output port 0 (register 04h) and the next byte will overwrite output port 1 (register 05h). Since every new write access after a STOP condition requires a command byte, which sets the pointer register, the next new write access will be to an arbitrary register.

There is no limit on the number of data bytes sent in one write transmission. In this way, the host can continuously update a register group independently of the other registers or the host can simply update a single register.

There are two 6-register groups: output drive strength (40h to 45h) and interrupt edge (60h to 65h) registers which can be programmed continuously in this group.

There is one register that is not part of a register group: output port configuration (5Ch). When this register is accessed multiple times, the register address remains fixed on the same address.

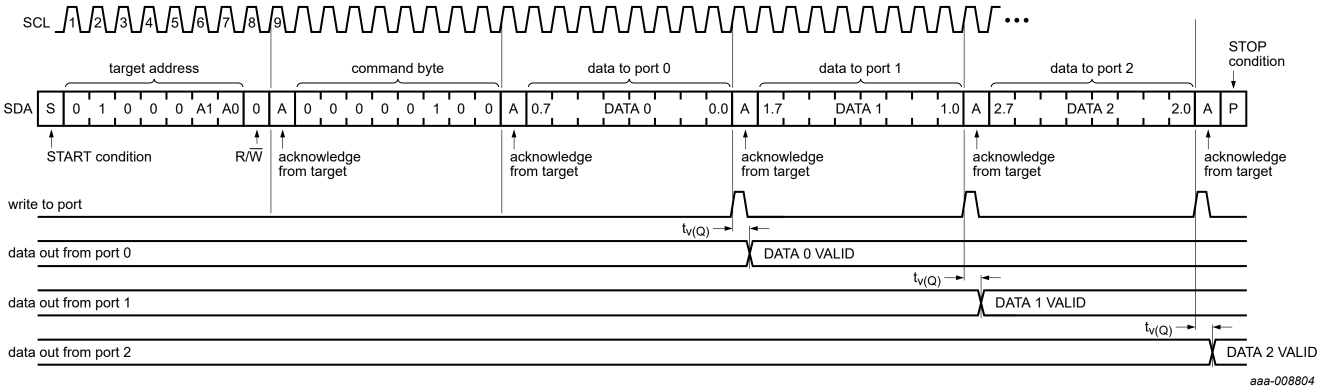


Figure 15. Write to output port register

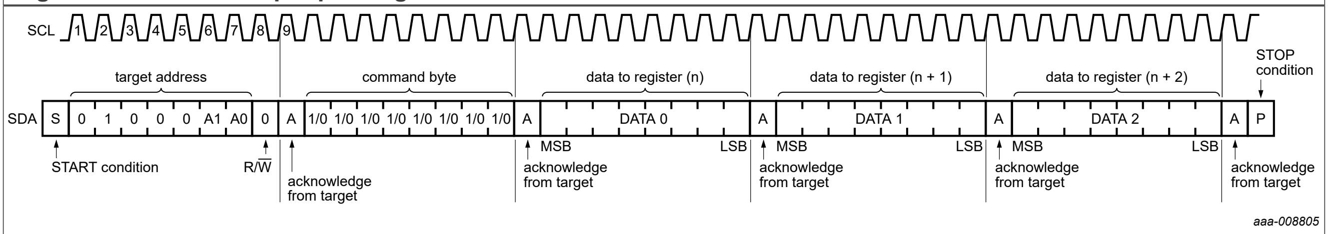


Figure 16. Write to device registers (operate as register triples)

7.2 Read commands

To read data from the PCAL6524 device, the bus controller must first send the PCAL6524 address with the least significant bit set to a logic 0 (for details on device address, see Figure 4). The command byte is sent after the address and determines which register is to be accessed.

After a restart or a STOP followed by a START condition, the device address is sent again. But this time, the least significant bit is set to a logic 1 to read data. Data from the register defined by the command byte is sent by the PCAL6524 (see Figure 17 to Figure 20). Additional bytes can be read after the first byte read is complete and reflects the next register in the group. For example, if input port 1 is read, the next byte read is input port 2. There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus controller must not acknowledge the data.

After a subsequent restart or a STOP followed by a START condition, the command byte contains the value of the next register to be read in the group. For example, if input port 1 was read last before the restart, the register that is read after the restart is the input port 2.

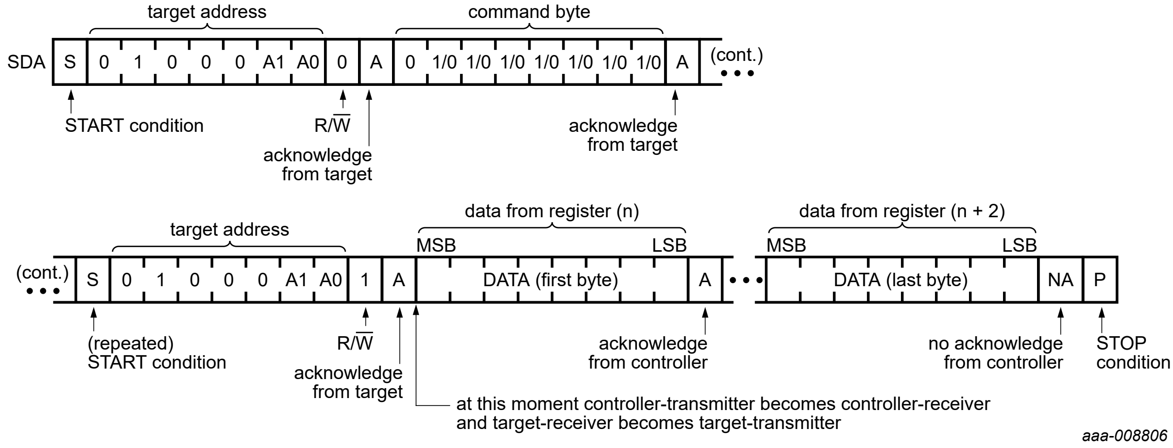
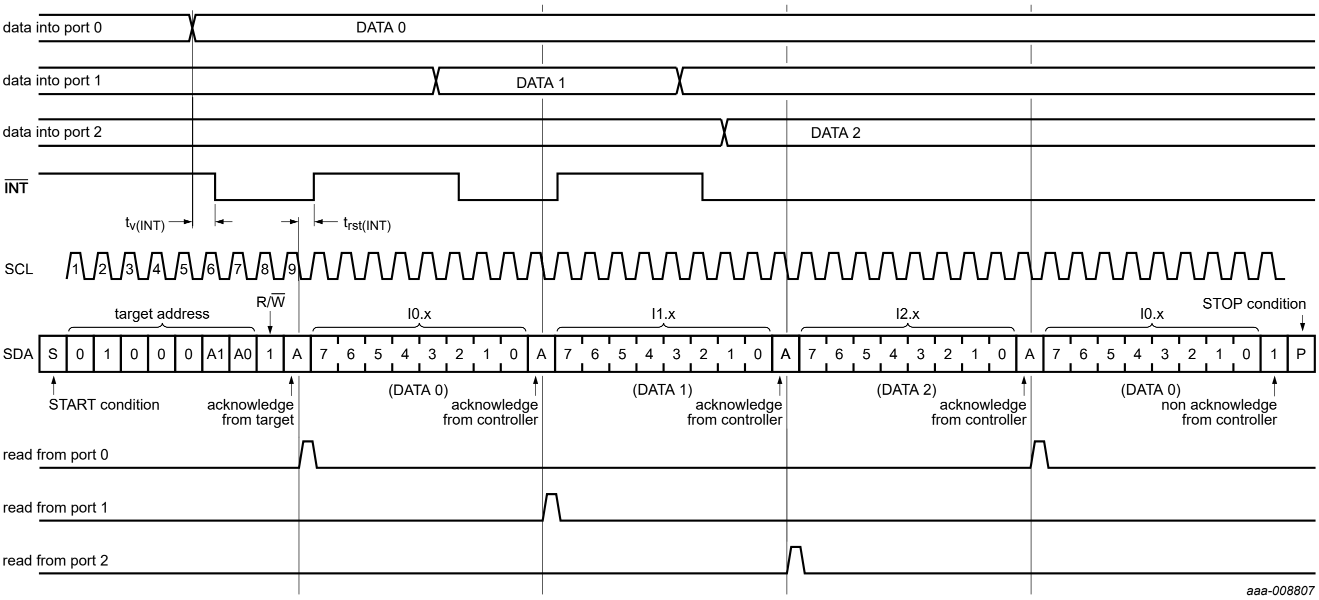


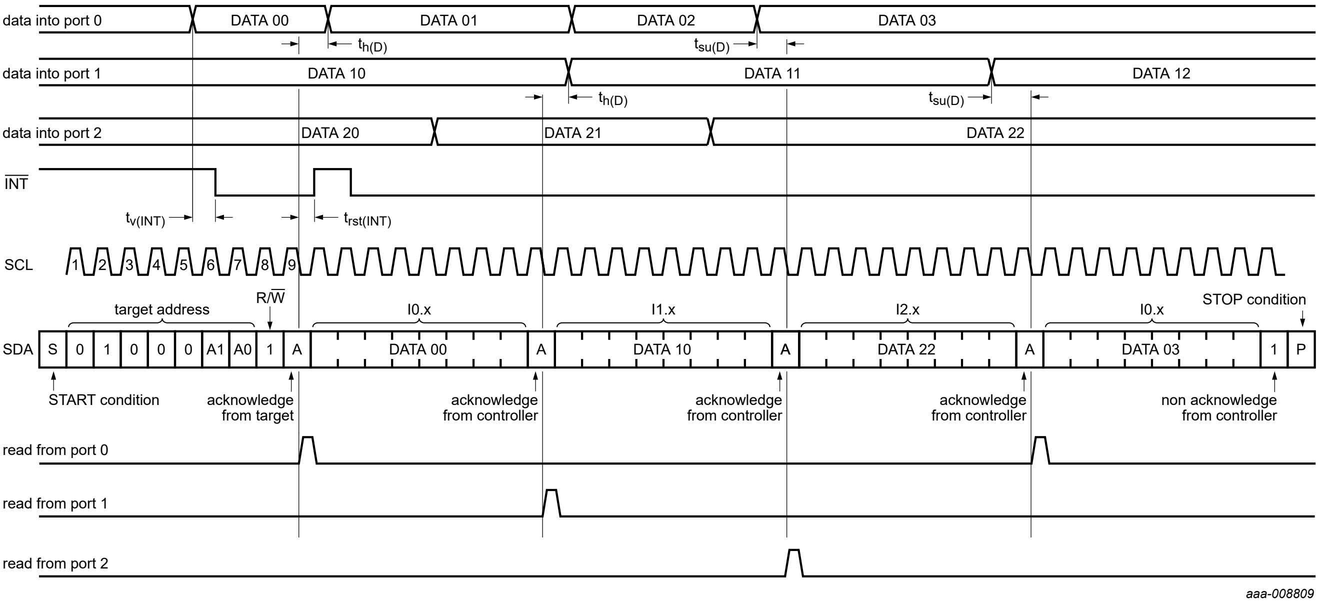
Figure 17. Read from device registers (operate as register triples)



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

This figure eliminates the command byte transfers and a restart between the initial target address call and actual data transfer from P port (for details, see Figure 17).

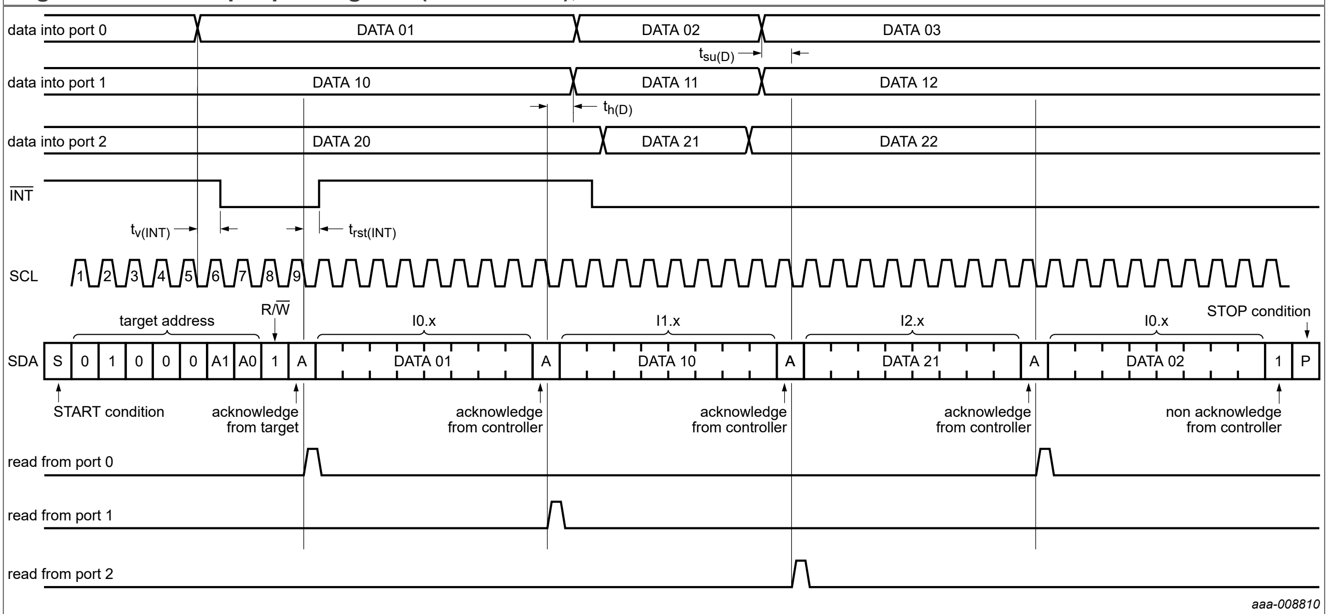
Figure 18. Read input port register (non-latched), scenario 1



Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

This figure eliminates the command byte transfers and a restart between the initial target address call and actual data transfer from P port (for details, see Figure 17).

Figure 19. Read input port register (non-latched), scenario 2



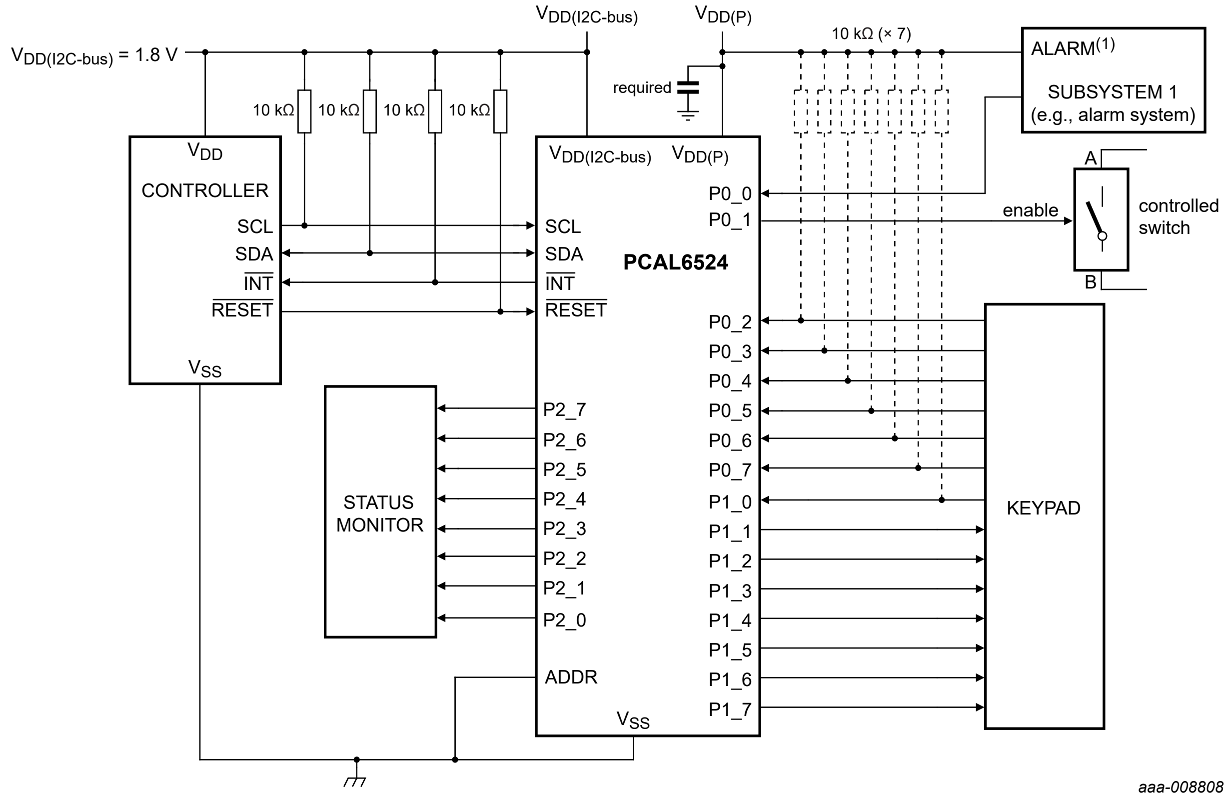
Remark: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

This figure eliminates the command byte transfers and a restart between the initial target address call and actual data transfer from P port (for details, see Figure 17).

Figure 20. Read input port register (latch enabled), scenario 3

8 Application design-in information

Figure 21 shows a typical application of PCAL6524.



Device address configured as 0100 010x for this example.

P0_0 and P0_2 through P1_0 are configured as inputs.

P0_1 and P1_1 through P1_7, and P2_0 through P2_7 are configured as outputs.

1. External resistors are required for inputs (on P port) that may float. If a driver to an input will never let the input float, a resistor is not needed with internal pull-up or pull-down resistor option. If an output in the P port is configured as an output, there is no need for external pull-up resistors.

Figure 21. Typical application

8.1 Output drive strength control

The output drive strength registers allow the user to control the output drive level of the GPIO. Each GPIO can be configured independently to one of the four possible output current levels. By programming these bits, the user is changing the number of transistor pairs or 'fingers' that drive the I/O pad.

Figure 22 shows a simplified output stage. The behavior of the pad is affected by the configuration register, the output port data, and the current control register. When the current control register bits are programmed to 01b, then only two of the fingers are active, reducing the current drive capability by 50 %.

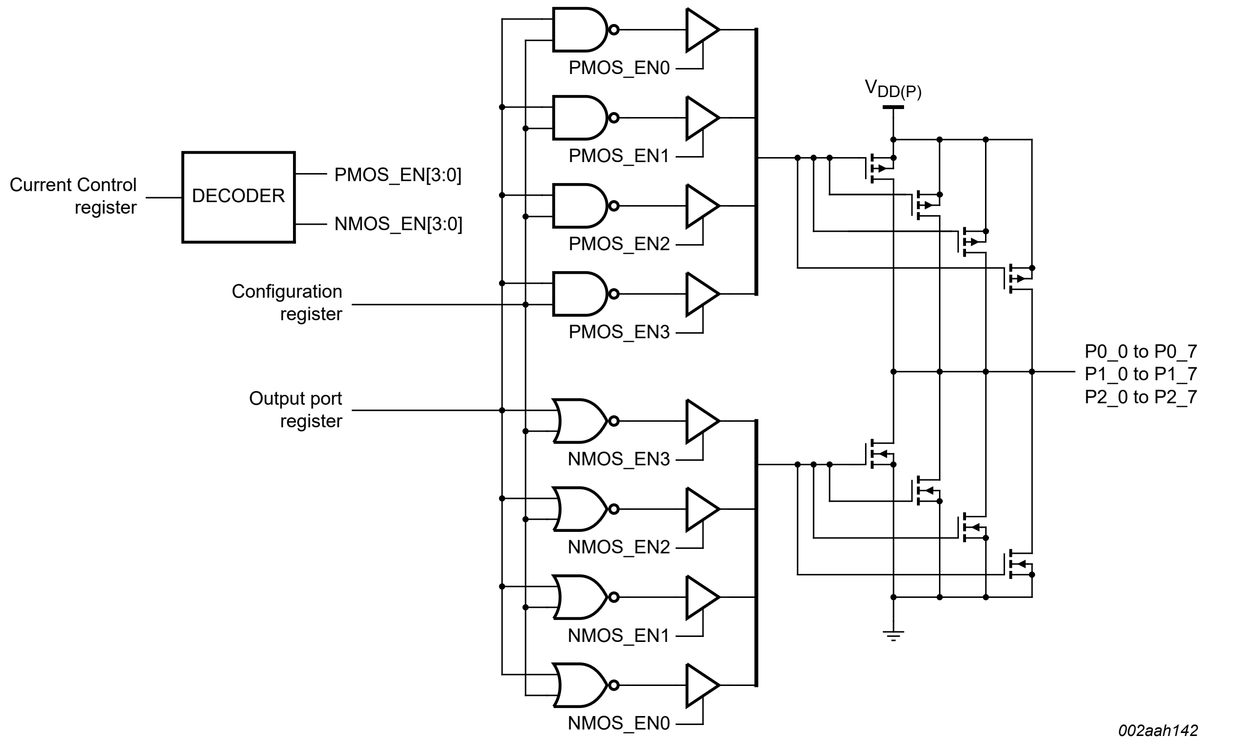


Figure 22. Simplified output stage

Reducing the current drive capability may be desirable to reduce system noise. When the output switches (transitions from H/L), there is a peak current that is a function of the output drive selection. This peak current runs through V_{DD} and V_{SS} package inductance and will create noise (some radiated, but more critically simultaneous switching noise (SSN)). In other words, switching many outputs at the same time will create ground and supply noise. The output drive strength control through the output drive strength registers allows the user to mitigate SSN issues without the need of additional external components.

In any case, a 0.1 uF bypass capacitor is required on the $V_{DD(P)}$ pin, located as close to the package as practical.

8.2 Power-on reset requirements

In the event of a glitch or data corruption, PCAL6524 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 23 and Figure 24.

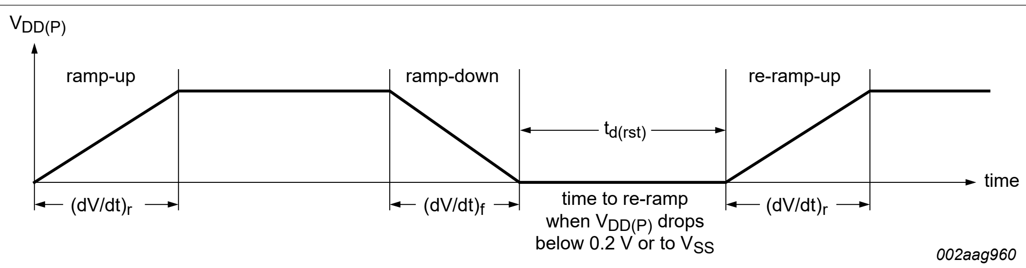


Figure 23. $V_{DD(P)}$ is lowered below 0.2 V or to 0 V and then ramped up to $V_{DD(P)}$

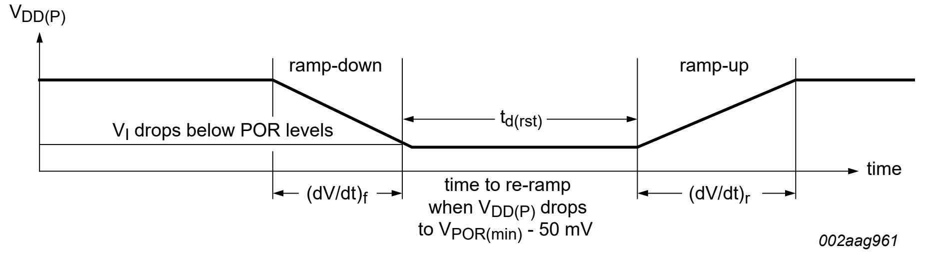


Figure 24. $V_{DD(P)}$ is lowered below the POR threshold, then ramped back up to $V_{DD(P)}$

Table 60 specifies the performance of the power-on reset feature for PCAL6524 for both types of power-on reset.

Table 60. Recommended supply sequencing and ramp rates

T_{amb} = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition		Min	Typ	Max	Unit
$(dV/dt)_f$	Fall rate of change of voltage	Figure 23		0.1	-	2000	ms
$(dV/dt)_r$	Rise rate of change of voltage	Figure 23		0.1	-	2000	ms
$t_{d(rst)}$	Reset delay time	Figure 23; re-ramp time when $V_{DD(P)}$ drops below 0.2 V or to V_{SS}		1	-	-	µs
		Figure 24; re-ramp time when $V_{DD(P)}$ drops to $V_{POR(min)}$ - 50 mV		1	-	-	µs
$\Delta V_{DD(gl)}$	Glitch supply voltage difference	Figure 25	[1]	-	-	1.0	V
$t_{w(gl)VDD}$	Supply voltage glitch pulse width	Figure 25	[2]	-	-	10	µs
$V_{POR(trip)}$	Power-on reset trip voltage	Falling $V_{DD(P)}$		0.7	-	-	V
		Rising $V_{DD(P)}$		-	-	1.5	V

[1] Level that $V_{DD(P)}$ can glitch down to with a ramp rate at 0.4 µs/V, but not cause a functional disruption when $t_{w(gl)VDD}$ < 1 µs.

[2] Glitch width that will not cause a functional disruption when $\Delta V_{DD(gl)} = 0.5 \times V_{DD(P)}$.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($t_{w(gl)VDD}$) and glitch height ($\Delta V_{DD(gl)}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 25 and Table 60 provide more information on how to measure these specifications.

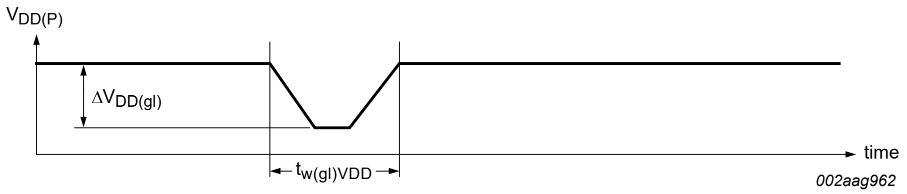


Figure 25. Glitch width and glitch height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^{2}C-bus/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{DD} being lowered to or from 0 V. Figure 26 and Table 60 provide more details on this specification.

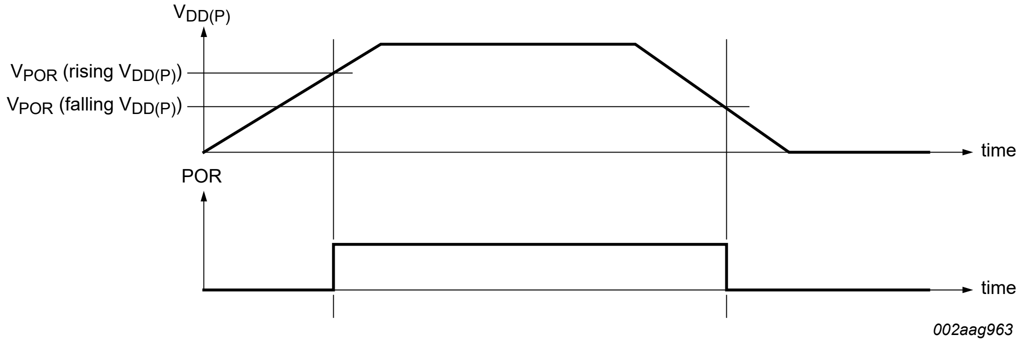


Figure 26. Power-on reset voltage (V_{POR})

8.3 Device current consumption with internal pull-up and pull-down resistors

The PCAL6524 integrates programmable pull-up and pull-down resistors to eliminate external components when pins are configured as inputs and pull-up or pull-down resistors are required (for example, nothing is driving the inputs to the power supply rails). Since these pull-up and pull-down resistors are internal to the device itself, they contribute to the current consumption of the device and must be considered in the overall system design.

The pull-up or pull-down function is selected in registers 50h, 51h, and 52h, while the resistor is connected by the enable registers 4Ch, 4Dh, and 4Eh. The configuration of the resistors is shown in Figure 11.

If the resistor is configured as a pull-up that is connected to V_{DD}, the current flows from the $V_{DD(P)}$ pin through the resistor to the ground when the pin is held LOW. The current appears as an additional I_{DD} upsetting any current consumption measurements.

In the same manner, if the resistor is configured as a pull-down and the pin is held HIGH, the current flows from the power supply through the pin to the V_{SS} pin. While this current will not be measured as part of I_{DD}, one must be mindful of the 200 mA limiting value through V_{SS}.

The pull-up and pull-down resistors are simple resistors and the current is linear with voltage. The resistance specification for these devices spans from 50 kΩ with a nominal 100 kΩ value. Any current flowing through these resistors is additive by the number of pins held HIGH or LOW and the current can be calculated by Ohm's law. See Figure 32 for a graph of supply current vs the number of pull-up resistors.

8.4 I²C-bus error recovery techniques

There are a number of techniques to recover from error conditions on the I²C-bus. Target devices like the PCAL6524 use a state machine to implement the I²C protocol and expect a certain sequence of events to occur to function properly. Unexpected events at the I²C controller can wreak havoc with the targets connected on the bus. However, it is possible to recover deterministically to a known bus state with careful protocol manipulation.

A hard target reset, either through power-on reset or by activating the $\overline{\text{RESET}}$ pin, sets the device back into the default state. This means the input/output pins and their configuration will be lost, which can cause some system issues.

A STOP condition, which is only initiated by the controller, resets the target state machine into a known condition where SDA is not driven LOW by the target. Logically, the target is waiting for a START condition. A STOP condition is defined as SDA transitioning from LOW to HIGH while SCL is HIGH.

If the controller is interrupted during a packet transmission, the target can send data or perform an acknowledge, driving the I²C-bus SDA line LOW. Since SDA is LOW, it effectively blocks any other I²C-bus transaction. A deterministic method to clear this situation, once the controller recognizes a 'stuck bus' state, is for the controller to blindly transmit nine clocks on SCL. If the target was transmitting data or acknowledging, nine or more clocks ensures the target state machine returns to a known, idle state since the protocol calls for eight data bits and one ACK bit. It does not matter when the target state machine finishes its transmission, extra clocks are recognized as STOP conditions.

The PCAL6524 SCL pin is an input only. If SCL is stuck LOW, then only the bus controller or a target performing a clock stretch operation can cause this condition.

With careful design of the bus controller error recovery firmware, many I²C-bus protocol problems can be avoided.

9 Limiting values

Table 61 describes the limiting values of PCAL6524.

Table 61. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(I2C-bus)}$	I²C-bus supply voltage			-0.5	+4.0	V
$V_{DD(P)}$	Supply voltage port P			-0.5	+6.5	V
$V_{I(P)}$	Input voltage on all ports		[1]	-0.5	+6.5	V
$V_{O(P)}$	Output voltage on all ports		[1]	-0.5	+6.5	V
$V_{I(I)}$	Input voltage on I²C-bus, $\overline{\text{RESET}}$, ADDR			-0.5	+4.0	V
$V_{O(I)}$	Output voltage on I²C-bus, $\overline{\text{INT}}$			-0.5	+4.0	V
I_{IK}	Input clamping current	ADDR, $\overline{\text{RESET}}$, SCL; $V_I < 0$ V		-	±20	mA
I_{OK}	Output clamping current	$\overline{\text{INT}}$; $V_O < 0$ V		-	±20	mA
I_{IOK}	Input/output clamping current	P port; $V_O < 0$ V or $V_O > V_{DD(P)}$		-	±20	mA
		SDA; $V_O < 0$ V or $V_O > V_{DD(I2C-bus)}$		-	±20	mA
I_{OL}	LOW-level output current	Continuous; P port; $V_O = 0$ V to $V_{DD(P)}$		-	50	mA
		Continuous; SDA, $\overline{\text{INT}}$; $V_O = 0$ V to $V_{DD(I2C-bus)}$		-	25	mA
I_{OH}	HIGH-level output current	Continuous; P port; $V_O = 0$ V to $V_{DD(P)}$		-	25	mA
I_{DD}	Supply current	Continuous through V_{SS}		-	200	mA
$I_{DD(P)}$	Supply current port P	Continuous through $V_{DD(P)}$		-	160	mA
$I_{DD(I2C-bus)}$	I²C-bus supply current	Continuous through $V_{DD(I2C-bus)}$		-	10	mA
T_{stg}	Storage temperature			-65	+150	°C
$T_{j(max)}$	Maximum junction temperature			-	125	°C

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

10 Recommended operating conditions

This section provides the recommended operation conditions for PCAL6524.

Table 62. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(I2C-bus)}$	I^2C-bus supply voltage		0.8	3.6	V
$V_{DD(P)}$	Supply voltage port P	A 0.1 μF bypass capacitor is required on $V_{DD(P)}$ pin as close to the package as practical	1.65	5.5	V
V_{IH}	HIGH-level input voltage	SCL, SDA, $\overline{RESET}$, ADDR			
		$V_{DD(I2C-bus)} \leq 1.1$ V	0.8 × $V_{DD(I2C-bus)}$	3.6	V
		$V_{DD(I2C-bus)} > 1.1$ V	0.7 × $V_{DD(I2C-bus)}$	3.6	V
		P2_7 to P0_0	0.7 × $V_{DD(P)}$	5.5	V
V_{IL}	LOW-level input voltage	SCL, SDA, $\overline{RESET}$, ADDR			
		$V_{DD(I2C-bus)} \leq 1.1$ V	-0.5	0.2 × $V_{DD(I2C-bus)}$	V
		$V_{DD(I2C-bus)} > 1.1$ V	-0.5	0.3 × $V_{DD(I2C-bus)}$	V
		P2_7 to P0_0	-0.5	0.3 × $V_{DD(P)}$	V
I_{OH}	HIGH-level output current	P2_7 to P0_0	-	10	mA
I_{OL}	LOW-level output current	P2_7 to P0_0	-	25	mA
T_{amb}	Ambient temperature	Operating in free air	-40	+85	°C

11 Thermal characteristics

Table 63 provides the thermal characteristics of PCAL6524.

Table 63. Thermal characteristics

Symbol	Parameter	Conditions	Value (typ)	Unit
$R_{th(j-a)}$	Thermal resistance from junction to ambient on a JEDEC 2S2P board[1]	HUQFN32 package	42	°C/W

[1] The package thermal resistance is calculated in accordance with JESD 51-7.

12 Static characteristics

Table 64 describes the static characteristics of PCAL6524.

Table 64. Static characteristics

T_{amb} = -40 °C to +85 °C; $V_{DD(I2C-bus)}$ = 0.8 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IK}	Input clamping voltage	I_I = -18 mA	-1.2	-	-	V
V_{POR}	Power-on reset voltage	$V_I = V_{DD(P)}$ or V_{SS}; I_O = 0 mA	-	1.2	1.5	V
V_{OH}	HIGH-level output voltage[2]	P port; I_{OH} = -8 mA; CCX.X = 11b				
		$V_{DD(P)}$ = 1.65 V	1.2	-	-	V
		$V_{DD(P)}$ = 2.3 V	1.8	-	-	V
		$V_{DD(P)}$ = 3 V	2.6	-	-	V
		$V_{DD(P)}$ = 4.5 V	4.1	-	-	V

Table 64. Static characteristics...*continued*

T_{amb} = -40 °C to +85 °C; $V_{DD(I2C-bus)}$ = 0.8 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
		P port; I_{OH} = -2.5 mA and CCX.X = 00b; I_{OH} = -5 mA and CCX.X = 01b; I_{OH} = -7.5 mA and CCX.X = 10b; I_{OH} = -10 mA and CCX.X = 11b;				
		$V_{DD(P)}$ = 1.65 V	1.1	-	-	V
		$V_{DD(P)}$ = 2.3 V	1.7	-	-	V
		$V_{DD(P)}$ = 3 V	2.5	-	-	V
		$V_{DD(P)}$ = 4.5 V	4.0	-	-	V
V_{OL}	LOW-level output voltage[2]	P port; I_{OL} = 8 mA; CCX.X = 11b				
		$V_{DD(P)}$ = 1.65 V	-	-	0.45	V
		$V_{DD(P)}$ = 2.3 V	-	-	0.25	V
		$V_{DD(P)}$ = 3 V	-	-	0.25	V
		$V_{DD(P)}$ = 4.5 V	-	-	0.20	V
		P port; I_{OL} = 2.5 mA and CCX.X = 00b; I_{OL} = 5 mA and CCX.X = 01b; I_{OL} = 7.5 mA and CCX.X = 10b; I_{OL} = 10 mA and CCX.X = 11b;				
		$V_{DD(P)}$ = 1.65 V	-	-	0.5	V
		$V_{DD(P)}$ = 2.3 V	-	-	0.3	V
		$V_{DD(P)}$ = 3 V	-	-	0.25	V
		$V_{DD(P)}$ = 4.5 V	-	-	0.2	V
I_{OL}	LOW-level output current[3]	SDA				
		V_{OL} = 0.4 V; $V_{DD(I2C-bus)} \leq 2$ V	15	-	-	mA
		V_{OL} = 0.4 V; $V_{DD(I2C-bus)} > 2$ V	20	-	-	mA
		$\overline{INT}$; V_{OL} = 0.4 V; $V_{DD(P)}$ = 1.65 V to 5.5 V	3	[4]	-	mA
I_I	Input current	ADDR, SCL, SDA, $\overline{RESET}$; $V_{DD(P)}$ = 1.65 V to 5.5 V; $V_I = V_{DD(I2C-bus)}$ or V_{SS}	-	-	±1	μA
I_{IH}	HIGH-level input current	P port; $V_I = V_{DD(P)}$; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	-	1	μA
I_{IL}	LOW-level input current	P port; $V_I = V_{SS}$; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	-	1	μA
I_{DD}	Supply current	Clocked mode; $I_{DD(I2C-bus)} + I_{DD(P)}$; SDA, P port, ADDR, $\overline{RESET}$; V_I on ADDR, SDA and $\overline{RESET} = V_{DD(I2C-bus)}$ or V_{SS}; V_I on P port = $V_{DD(P)}$; I_O = 0 mA; I/O = inputs				
		$V_{DD(P)}$ = 3.6 V to 5.5 V; f_{SCL} = 0 kHz	-	3	7	μA
		$V_{DD(P)}$ = 2.3 V to 3.6 V; f_{SCL} = 0 kHz	-	2	5	μA
		$V_{DD(P)}$ = 1.65 V to 2.3 V; f_{SCL} = 0 kHz	-	1.5	3	μA
		$V_{DD(P)}$ = 3.6 V to 5.5 V; f_{SCL} = 400 kHz	-	27	45	μA
		$V_{DD(P)}$ = 2.3 V to 3.6 V; f_{SCL} = 400 kHz	-	12	25	μA

Table 64. Static characteristics...*continued*

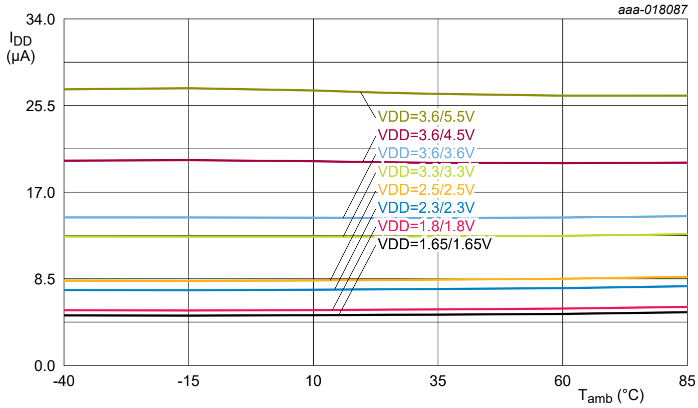
T_{amb} = -40 °C to +85 °C; $V_{DD(I2C\text{-}bus)}$ = 0.8 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
		$V_{DD(P)}$ = 1.65 V to 2.3 V; f_{SCL} = 400 kHz	-	7.5	15	μA
		$V_{DD(P)}$ = 3.6 V to 5.5 V; f_{SCL} = 1 MHz	-	70	110	μA
		$V_{DD(P)}$ = 2.3 V to 3.6 V; f_{SCL} = 1 MHz	-	30	60	μA
		$V_{DD(P)}$ = 1.65 V to 2.3 V; f_{SCL} = 1 MHz	-	20	40	μA
		Active mode; $I_{DD(I2C\text{-}bus)} + I_{DD(P)}$; P port, ADDR, $\overline{RESET}$; V_I on ADDR, $\overline{RESET}$ = $V_{DD(I2C\text{-}bus)}$; V_I on P port = $V_{DD(P)}$; I_O = 0 mA; I/O = inputs; continuous register read				
		$V_{DD(P)}$ = 3.6 V to 5.5 V; f_{SCL} = 400 kHz	-	150	250	μA
		$V_{DD(P)}$ = 2.3 V to 3.6 V; f_{SCL} = 400 kHz	-	120	200	μA
		$V_{DD(P)}$ = 1.65 V to 2.3 V; f_{SCL} = 400 kHz	-	75	150	μA
		$V_{DD(P)}$ = 3.6 V to 5.5 V; f_{SCL} = 1 MHz	-	450	625	μA
		$V_{DD(P)}$ = 2.3 V to 3.6 V; f_{SCL} = 1 MHz	-	270	500	μA
		$V_{DD(P)}$ = 1.65 V to 2.3 V; f_{SCL} = 1 MHz	-	160	210	μA
		With pull-ups enabled; $I_{DD(I2C\text{-}bus)} + I_{DD(P)}$; P port, ADDR, $\overline{RESET}$; V_I on ADDR, SCL, SDA and $\overline{RESET}$ = $V_{DD(I2C\text{-}bus)}$ or V_{SS}; V_I on P port = V_{SS}; I_O = 0 mA; I/O = inputs with pull-up enabled; f_{SCL} = 0 kHz				
		$V_{DD(P)}$ = 1.65 V to 5.5 V	-	1.7	2.5	mA
ΔI_{DD}	Additional quiescent supply current[5]	ADDR, SCL, SDA, $\overline{RESET}$; one input at $V_{DD(I2C\text{-}bus)}$ - 0.6 V, other inputs at $V_{DD(I2C\text{-}bus)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	-	25	μA
		P port; one input at $V_{DD(P)}$ - 0.6 V, other inputs at $V_{DD(P)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	-	80	μA
C_i	Input capacitance[6]	V_I = $V_{DD(I2C\text{-}bus)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	6	-	pF
C_{io}	Input/output capacitance[7]	$V_{I/O}$ = $V_{DD(I2C\text{-}bus)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	7	-	pF
		$V_{I/O}$ = $V_{DD(P)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V	-	7.5	-	pF
$R_{pu(int)}$	Internal pull-up resistance	Input/output	50	100	150	kΩ
$R_{pd(int)}$	Internal pull-down resistance	Input/output	50	100	150	kΩ

[1] For I_{DD}, all typical values are at nominal supply voltage (1.8 V, 2.5 V, 3.3 V, or 3.6 V V_{DD}) and T_{amb} = 25 °C. Except for I_{DD}, the typical values are at $V_{DD(P)}$ = $V_{DD(I2C\text{-}bus)}$ = 3.3 V and T_{amb} = 25 °C.
[2] The total current sourced by all I/Os must be limited to 160 mA.
[3] Each I/O must be externally limited to a maximum of 25 mA and each octal (P0_0 to P0_7 and P1_0 to P1_7) must be limited to a maximum current of 100 mA, for a device total of 200 mA.
[4] Typical value for T_{amb} = 25 °C. V_{OL} = 0.4 V and $V_{DD(I2C\text{-}bus)}$ = $V_{DD(P)}$ = 3.3 V. Typical value for $V_{DD(I2C\text{-}bus)}$ = $V_{DD(P)}$ < 2.5 V, V_{OL} = 0.6 V.
[5] Internal pull-up/pull-down resistors disabled.
[6] Value is not tested in production, but guaranteed by design and characterization.
[7] Value not tested in production, but guaranteed by design and characterization.

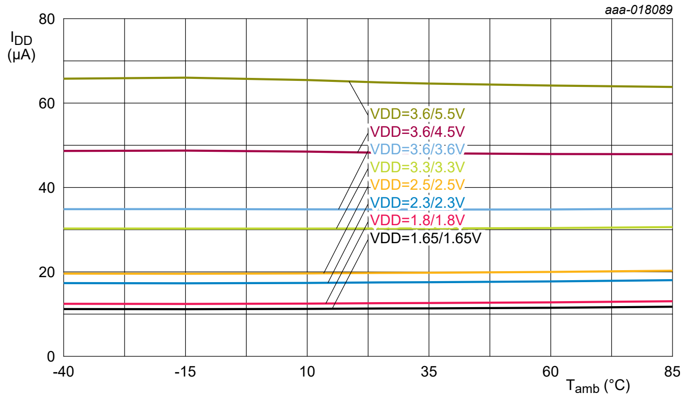
12.1 Typical characteristics

Figures given below describe the typical characteristics of PCAL6524.



a. SCL = 400 kHz

Figure 27. Supply current vs ambient temperature



b. SCL = 1 MHz

Figure 28. Supply current vs ambient temperature

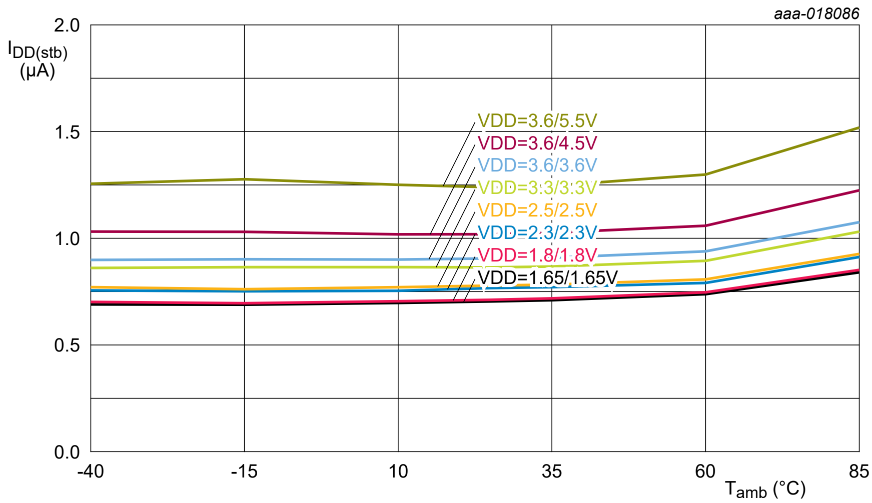
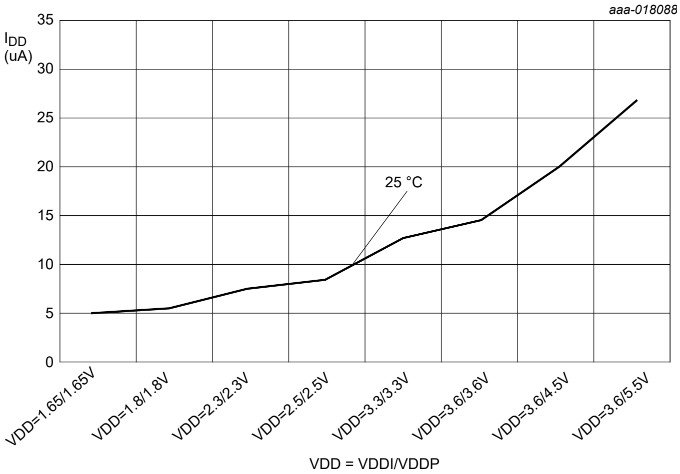
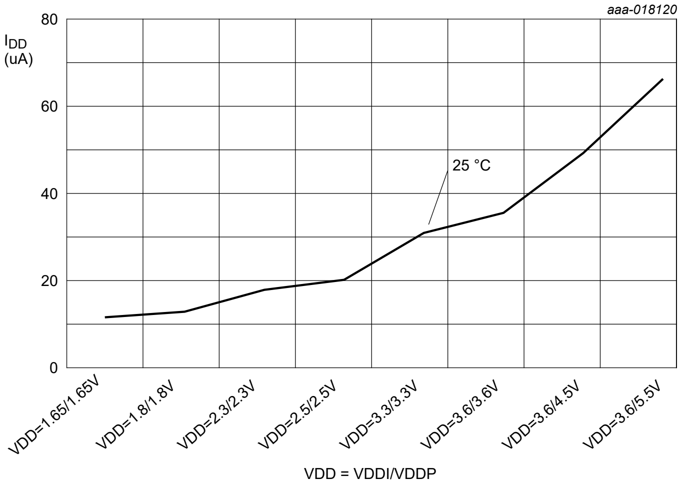


Figure 29. Standby supply current vs ambient temperature



a. SCL = 400 kHz

Figure 30. Supply current vs supply voltage



b. SCL = 1 MHz

Figure 31. Supply current vs supply voltage

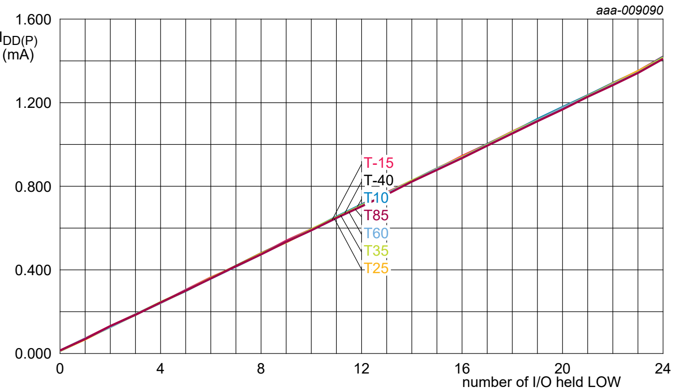
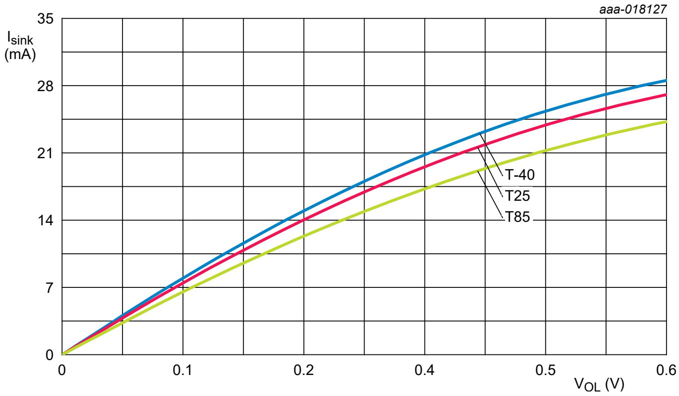
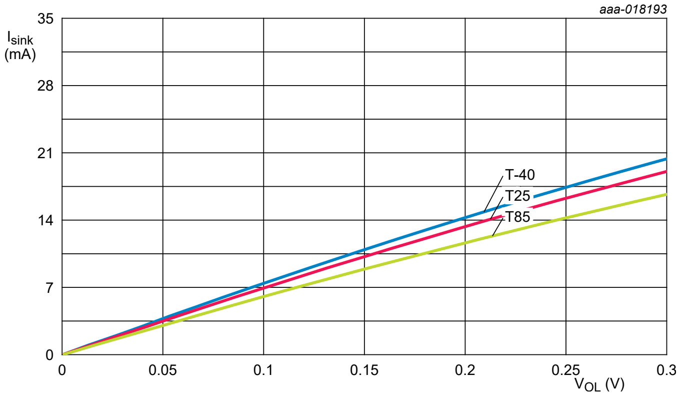


Figure 32. Supply current vs number of I/O held LOW



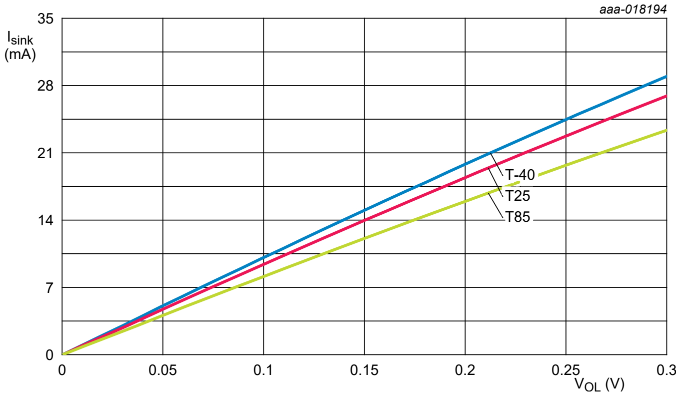
a. $V_{DD(P)}$ = 1.65 V

Figure 33. I/O sink current vs LOW-level output voltage



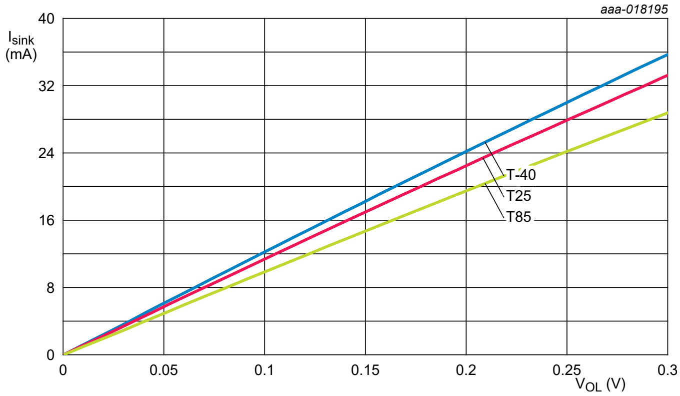
b. $V_{DD(P)}$ = 1.8 V

Figure 34. I/O sink current vs LOW-level output voltage



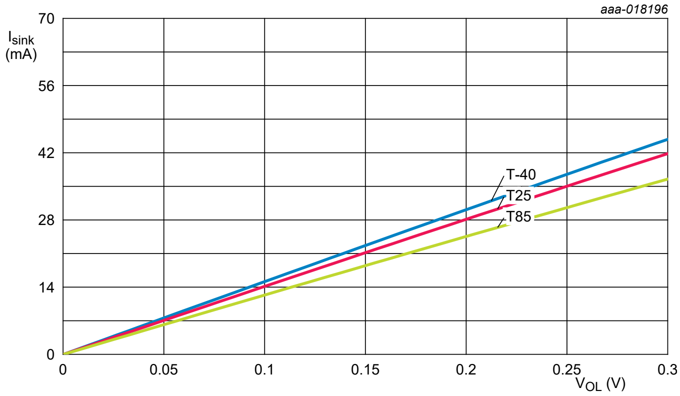
c. $V_{DD(P)}$ = 2.5 V

Figure 35. I/O sink current vs LOW-level output voltage



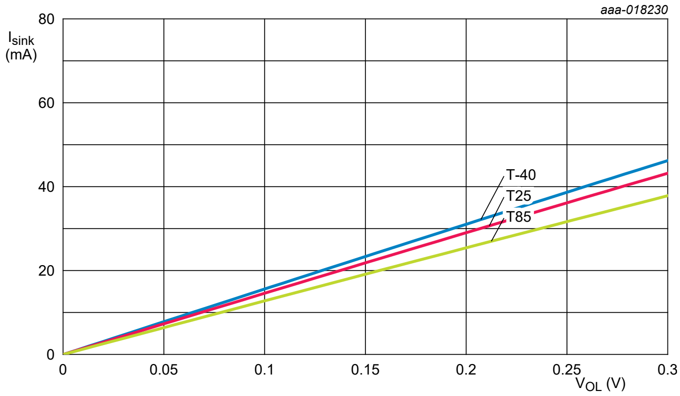
d. $V_{DD(P)}$ = 3.3 V

Figure 36. I/O sink current vs LOW-level output voltage



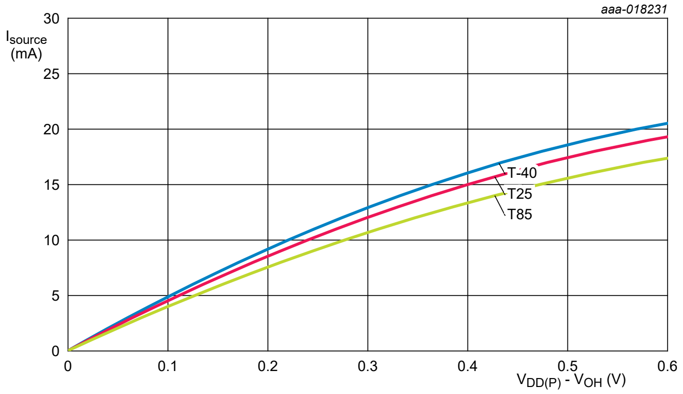
e. $V_{DD(P)}$ = 5 V

Figure 37. I/O sink current vs LOW-level output voltage



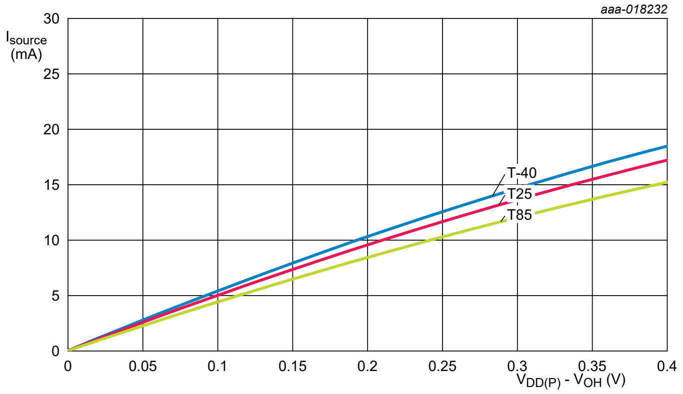
f. $V_{DD(P)}$ = 5.5 V

Figure 38. I/O sink current vs LOW-level output voltage



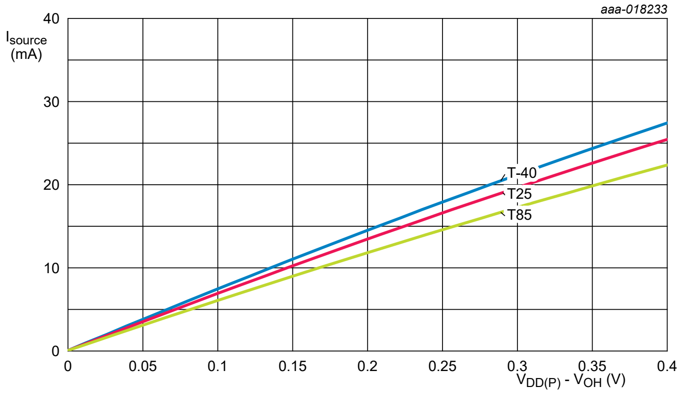
a. $V_{DD(P)}$ = 1.65 V

Figure 39. I/O source current vs HIGH-level output voltage



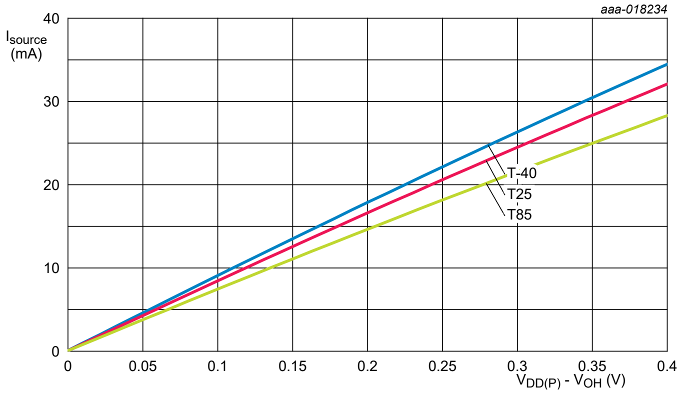
b. $V_{DD(P)}$ = 1.8 V

Figure 40. I/O source current vs HIGH-level output voltage



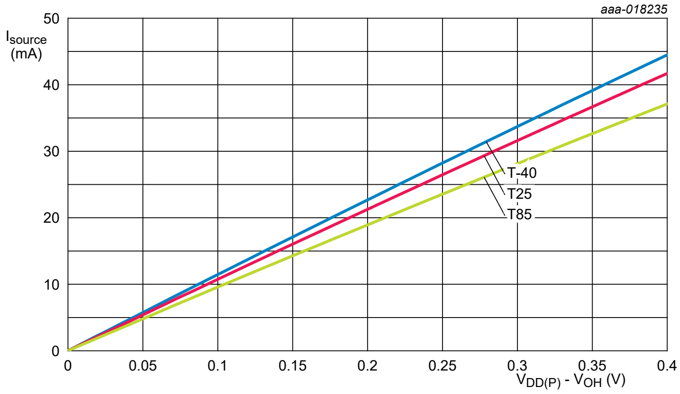
c. $V_{DD(P)}$ = 2.5 V

Figure 41. I/O source current vs HIGH-level output voltage



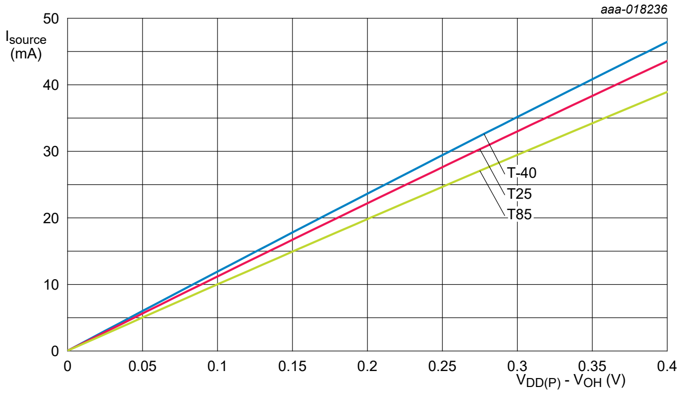
d. $V_{DD(P)}$ = 3.3 V

Figure 42. I/O source current vs HIGH-level output voltage



e. $V_{DD(P)}$ = 5 V

Figure 43. I/O source current vs HIGH-level output voltage



f. $V_{DD(P)}$ = 5.5 V

Figure 44. I/O source current vs HIGH-level output voltage

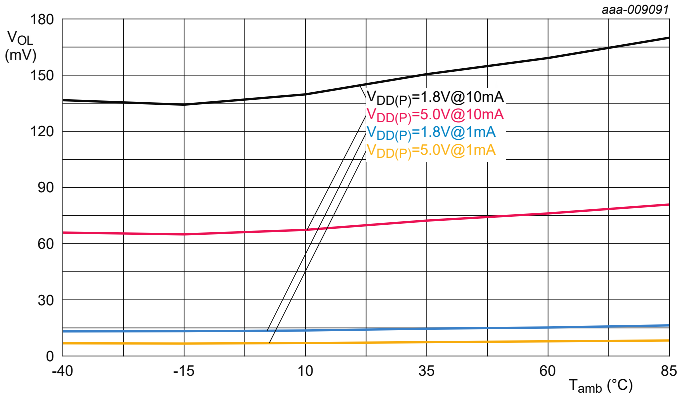


Figure 45. LOW-level output voltage vs temperature

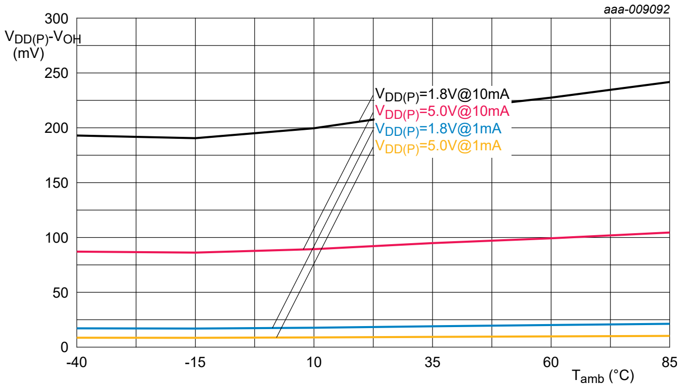


Figure 46. I/O high voltage vs temperature

13 Dynamic characteristics

This section describes the dynamic characteristics of PCAL6524. It is organized into three tables as follows:

Table 65. I²C-bus interface timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Figure 48.

Symbol	Parameter	Conditions		Standard-mode I²C-bus		Fast-mode I²C-bus		Fast-mode Plus I²C-bus		Unit
				Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency			0	100	0	400	0	1000	kHz
t_{HIGH}	HIGH period of the SCL clock			4	-	0.6	-	0.26	-	μs
t_{LOW}	LOW period of the SCL clock			4.7	-	1.3	-	0.5	-	μs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter			0	50	0	50	0	50	ns
$t_{SU;DAT}$	Data set-up time			250	-	100	-	50	-	ns
$t_{HD;DAT}$	Data hold time			0	-	0	-	0	-	ns
t_r	Rise time of both SDA and SCL signals		[1]	-	1000	20	300	-	120	ns

Table 65. I²C-bus interface timing requirements*...continued*

Over recommended operating free air temperature range, unless otherwise specified. See Figure 48.

Symbol	Parameter	Conditions		Standard-mode I²C-bus		Fast-mode I²C-bus		Fast-mode Plus I²C-bus		Unit
				Min	Max	Min	Max	Min	Max	
t_f	Fall time of both SDA and SCL signals		[1]	-	300	20 × (V_{DD} / 5.5 V)	300	-	120	ns
t_{BUF}	Bus free time between a STOP and START condition			4.7	-	1.3	-	0.5	-	μs
$t_{SU;STA}$	Set-up time for a repeated START condition			4.7	-	0.6	-	0.26	-	μs
$t_{HD;STA}$	Hold time (repeated) START condition			4	-	0.6	-	0.26	-	μs
$t_{SU;STO}$	Set-up time for STOP condition			4	-	0.6	-	0.26	-	μs
$t_{VD;DAT}$	Data valid time	SCL LOW to SDA output valid		-	3.45	-	0.9	-	0.45	μs
$t_{VD;ACK}$	Data valid acknowledge time	ACK signal from SCL LOW to SDA (out) LOW		-	3.45	-	0.9	-	0.45	μs

[1] Value is not tested in production, but guaranteed by design and characterization.

Table 66. Reset timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Figure 50.

Symbol	Parameter	Conditions		Standard-mode I²C-bus		Fast-mode I²C-bus		Fast-mode Plus I²C-bus		Unit
				Min	Max	Min	Max	Min	Max	
$t_{w(rst)}$	Reset pulse width			150	-	150	-	150	-	ns
$t_{rec(rst)}$	Reset recovery time			500	-	500	-	500	-	ns
t_{rst}	Reset time		[1]	600	-	600	-	600	-	ns

[1] Minimum time for SDA to become HIGH or minimum time to wait before doing a START.

Table 67. Switching characteristics

Over recommended operating free air temperature range; $C_L \leq 100$ pF; unless otherwise specified. See Figure 49.

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Fast-mode Plus I2C-bus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{v(INT)}$	Valid time on pin $\overline{INT}$	From P port to $\overline{INT}$	-	1	-	1	-	1	μs
$t_{rst(INT)}$	Reset time on pin $\overline{INT}$	From SCL to $\overline{INT}$	-	1	-	1	-	1	μs

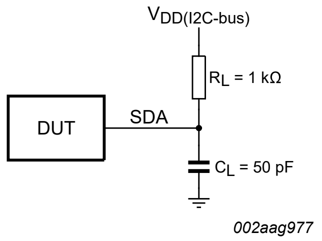
Table 67. Switching characteristics*...continued*

Over recommended operating free air temperature range; $C_L \leq 100$ pF; unless otherwise specified. See Figure 49.

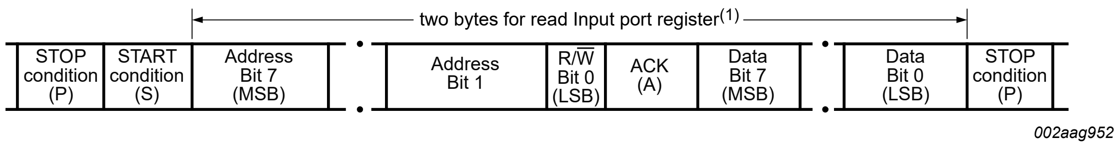
Symbol	Parameter	Conditions	Standard-mode I^2C-bus		Fast-mode I^2C-bus		Fast-mode Plus I2C-bus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{v(Q)}$	Data output valid time	From SCL to P port	-	400	-	400	-	400	ns
$t_{su(D)}$	Data input set-up time	From P port to SCL	0	-	0	-	0	-	ns
$t_{h(D)}$	Data input hold time	From P port to SCL	300	-	300	-	300	-	ns

14 Parameter measurement information

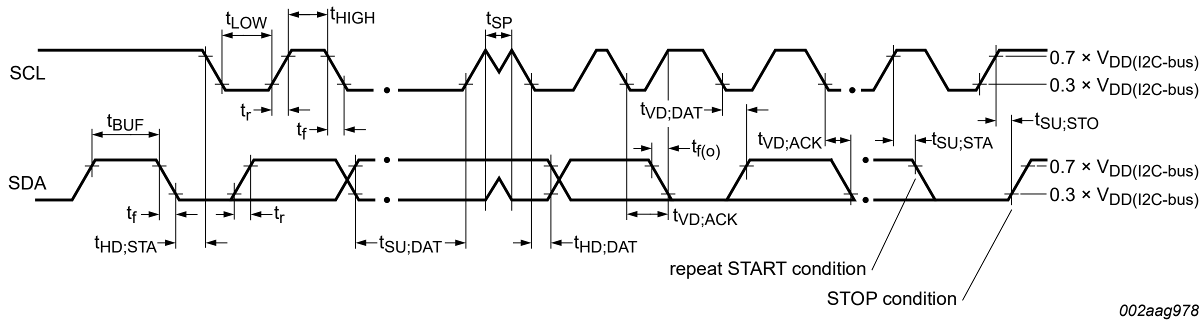
This section covers the parameter measurement information, including load circuits and voltage waveforms for key interfaces and signals.



a. SDA load configuration



b. Transaction format



c. Voltage waveforms

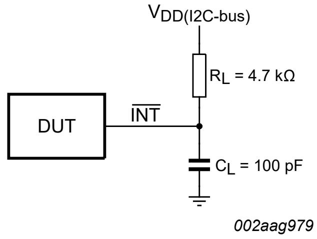
C_L includes probe and jig capacitance.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; $Z_o = 50\ \Omega$; $t_r/t_f \leq 30$ ns.

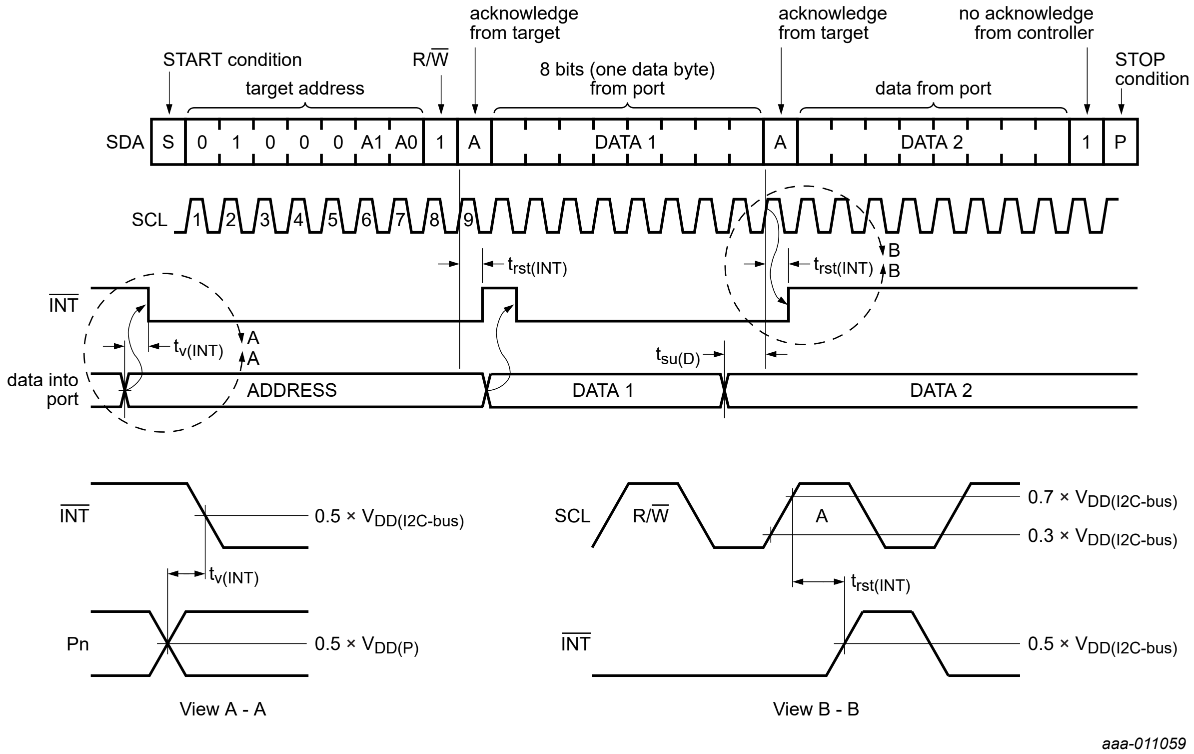
All parameters and waveforms are not applicable to all devices.

Byte 1 = I^2C-bus address; Byte 2, byte 3 = P port data.

Figure 47. I^2C-bus interface load circuit and voltage waveforms



a. Interrupt load configuration



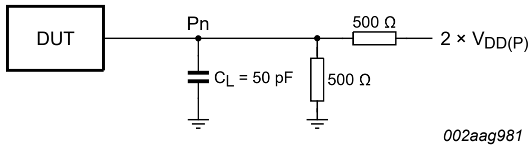
b. Voltage waveforms

C_L includes probe and jig capacitance.

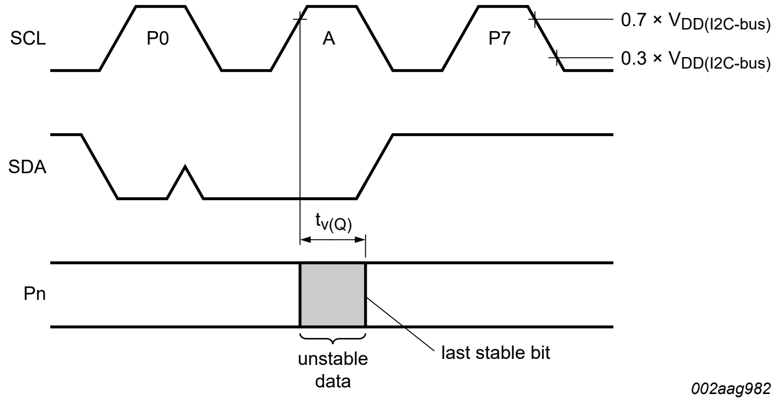
All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

All parameters and waveforms are not applicable to all devices.

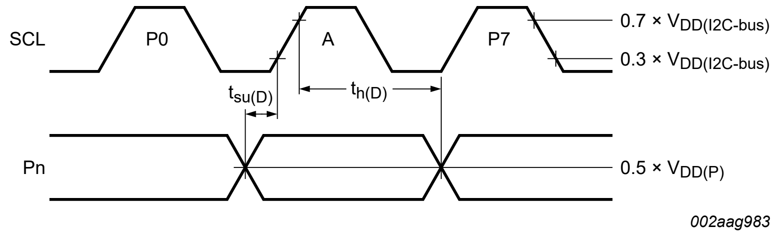
Figure 48. Interrupt load circuit and voltage waveforms



a. P port load configuration



b. Write mode (R/$\overline{\text{W}}$ = 0)



c. Read mode (R/$\overline{\text{W}}$ = 1)

C_L includes probe and jig capacitance.

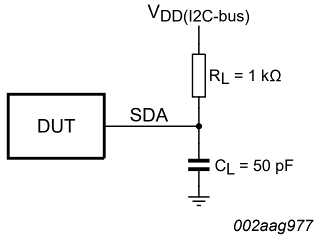
$t_{v(Q)}$ is measured from 0.7 × $V_{DD(I2C\text{-}bus)}$ on SCL to 50 % I/O (Pn) output.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

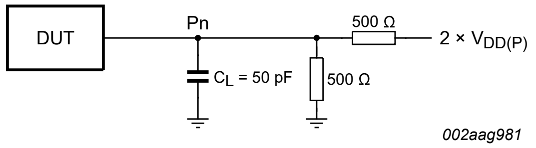
The outputs are measured one at a time, with one transition per measurement.

All parameters and waveforms are not applicable to all devices.

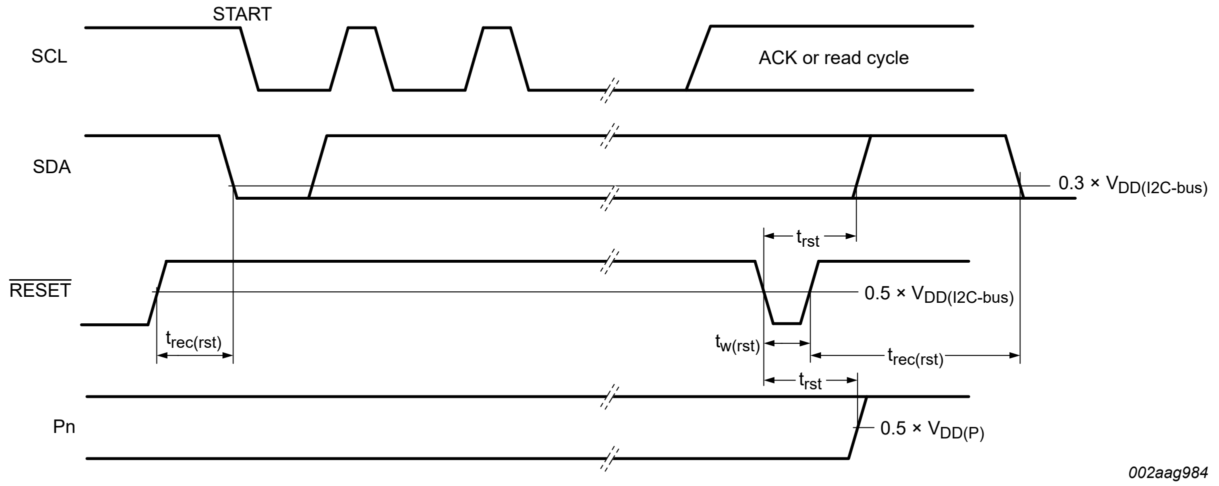
Figure 49. P port load circuit and voltage waveforms



a. SDA load configuration



b. P port load configuration



c. RESET timing

C_L includes probe and jig capacitance.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

The outputs are measured one at a time, with one transition per measurement.

I/Os are configured as inputs.

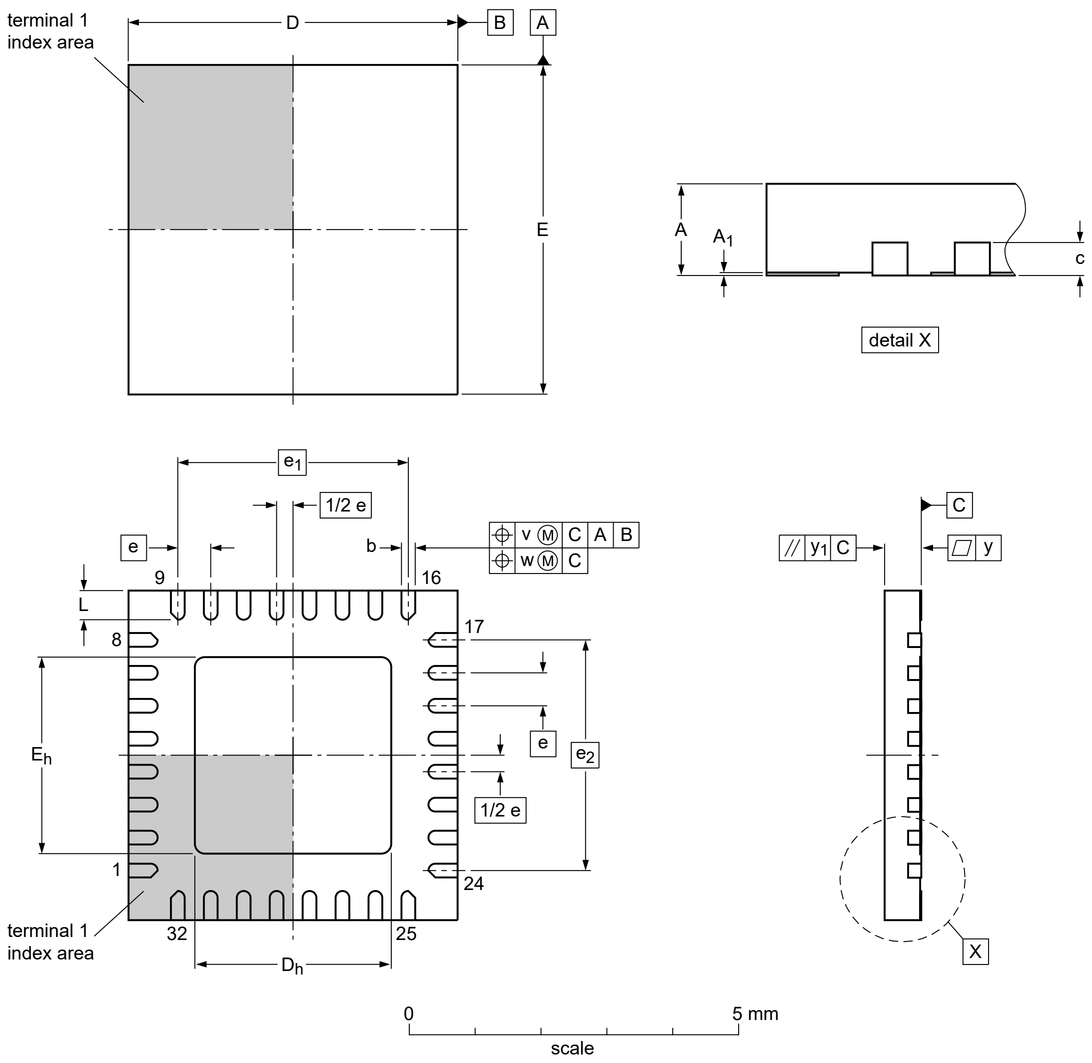
All parameters and waveforms are not applicable to all devices.

Figure 50. Reset load circuits and voltage waveforms

15 Package outline

This section covers the package outlines for SOT1426-1 (HUQFN32) and SOT1851-1 (VFBGA36).

HUQFN32: plastic thermal enhanced ultra thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.56 mm **SOT1426-1**



Dimensions (mm are the original dimensions)

Unit		A(1)	A_1	b	C	D	D_h	E	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	0.60	0.05	0.30		5.1	3.1	5.1	3.1				0.45				
mm	nom	0.56	0.02	0.21	0.2	5.0	3.0	5.0	3.0	0.5	3.5	3.5	0.40	0.1	0.05	0.05	0.1
	min	0.45	0.00	0.18		4.9	2.9	4.9	2.9				0.35				

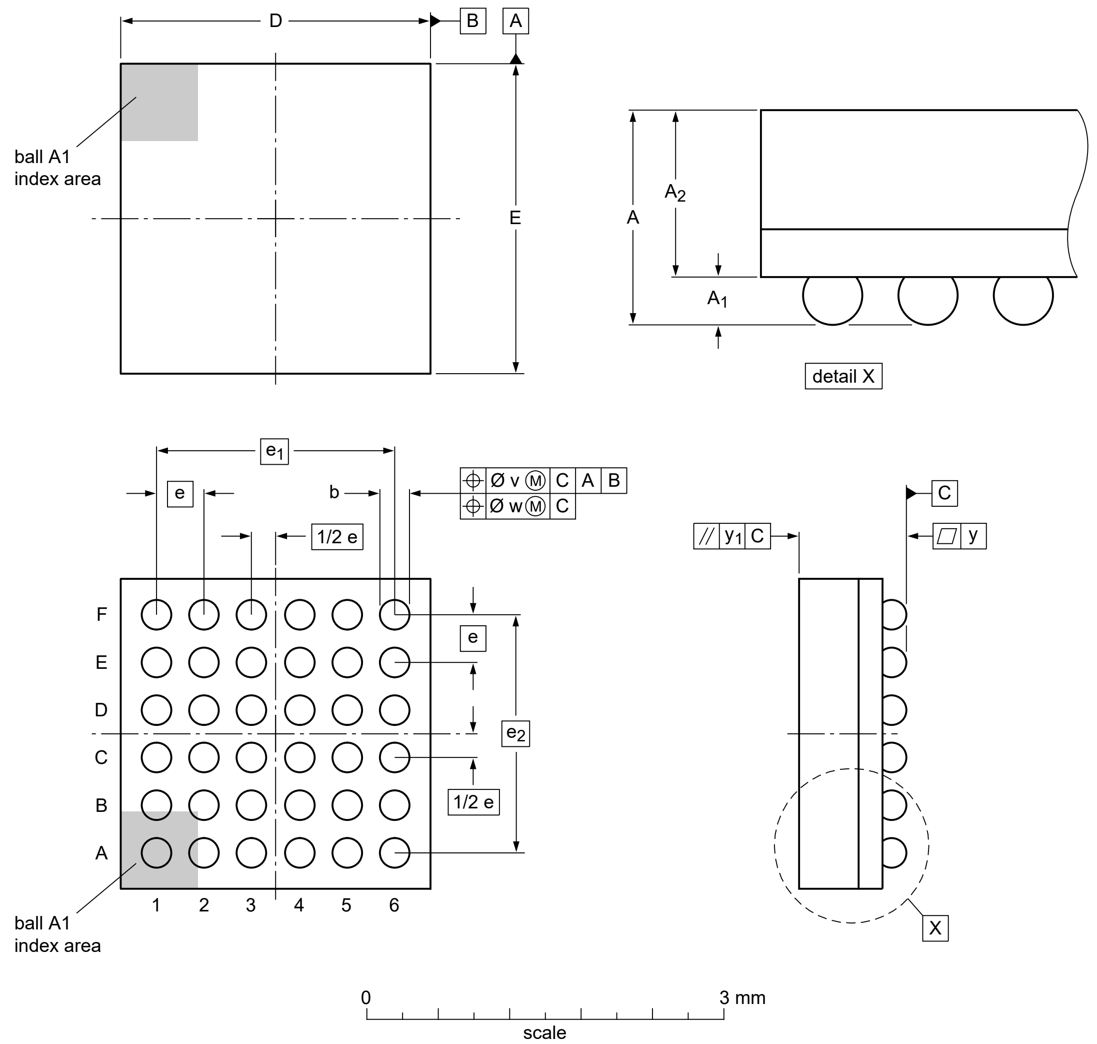
Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1426-1_po

Outline version	References: IEC	References: JEDEC	References: JEITA		European projection	Issue date
SOT1426-1						~~14-08-06~~ 14-08-07

Figure 51. Package outline SOT1426-1 (HUQFN32)

VFBGA36: plastic very thin fine-pitch ball grid array package; 36 balls **SOT1851-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
	max	1.00	0.25	0.75	0.30	2.70	2.70							
mm	nom	0.90	0.20	0.70	0.25	2.60	2.60	0.4	2.0	2.0	0.15	0.05	0.08	0.1
	min	0.80	0.15	0.65	0.20	2.50	2.50							

sot1851-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
sot1851-1	- - -					~~15-12-14~~ 16-02-08

Figure 52. Package outline SOT1851-1 (VFBGA36)

16 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 53) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 68 and Table 69

Table 68. SnPb eutectic process (from J-STD-020D)

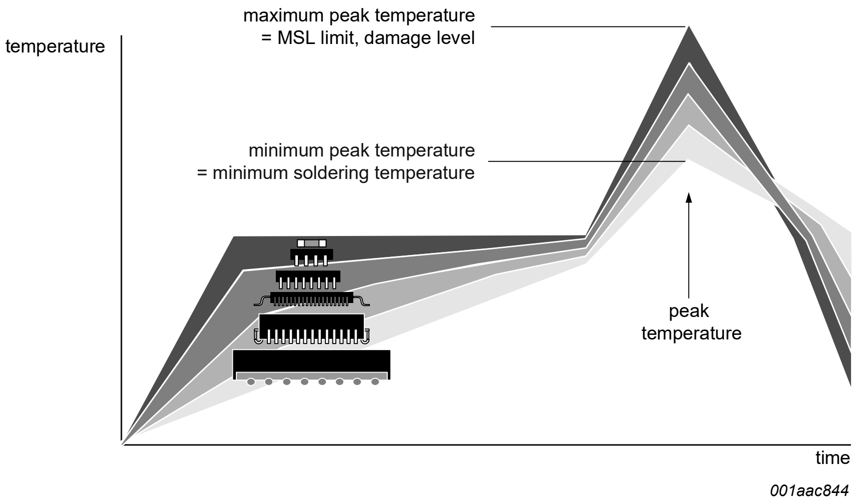
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 69. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 53.



MSL: Moisture Sensitivity Level

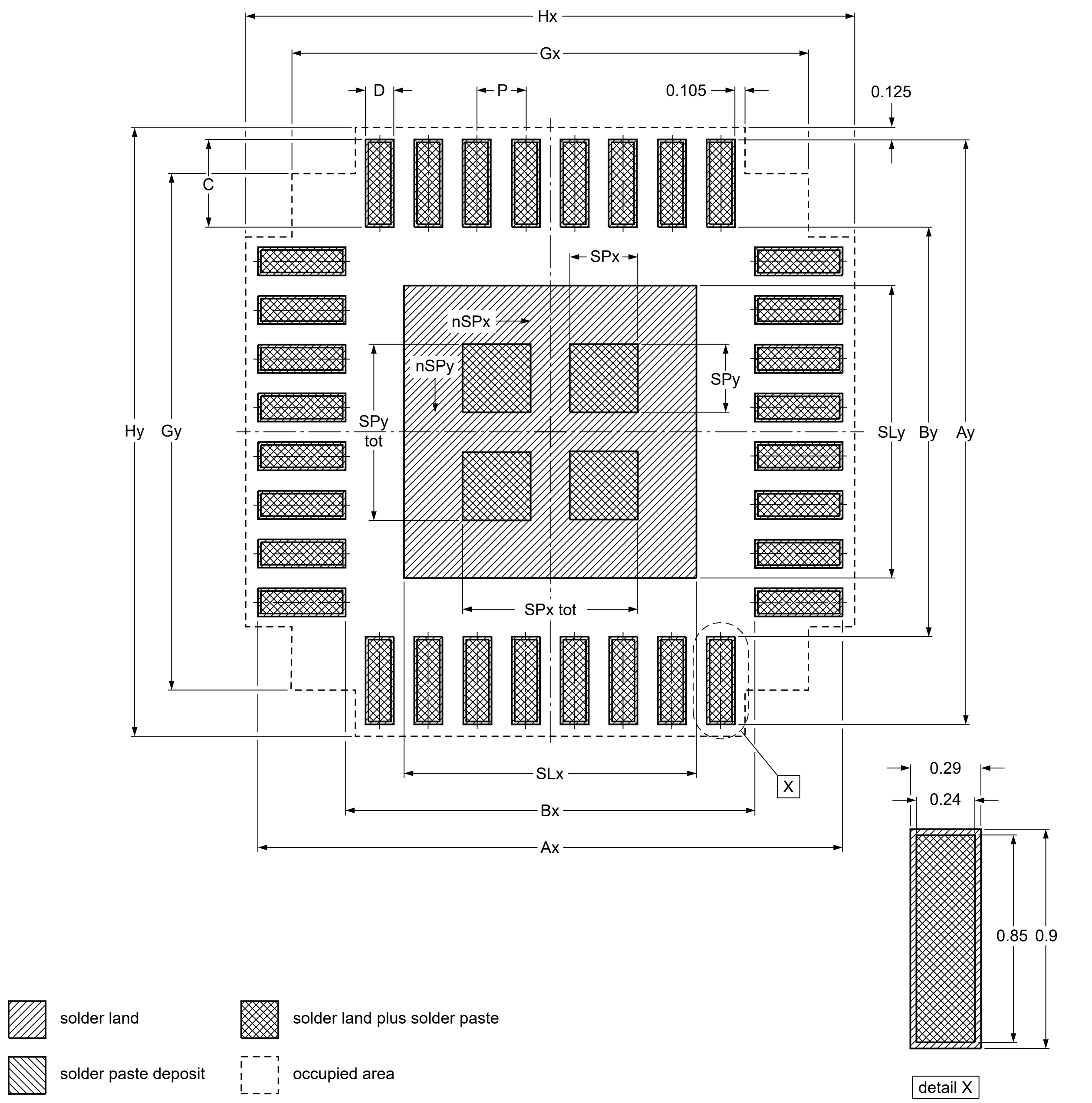
Figure 53. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

17 Soldering: PCB footprints

This section provides figures of PCB footprints for soldering operation.

Footprint information for reflow soldering of HUQFN32 package **SOT1426-1**



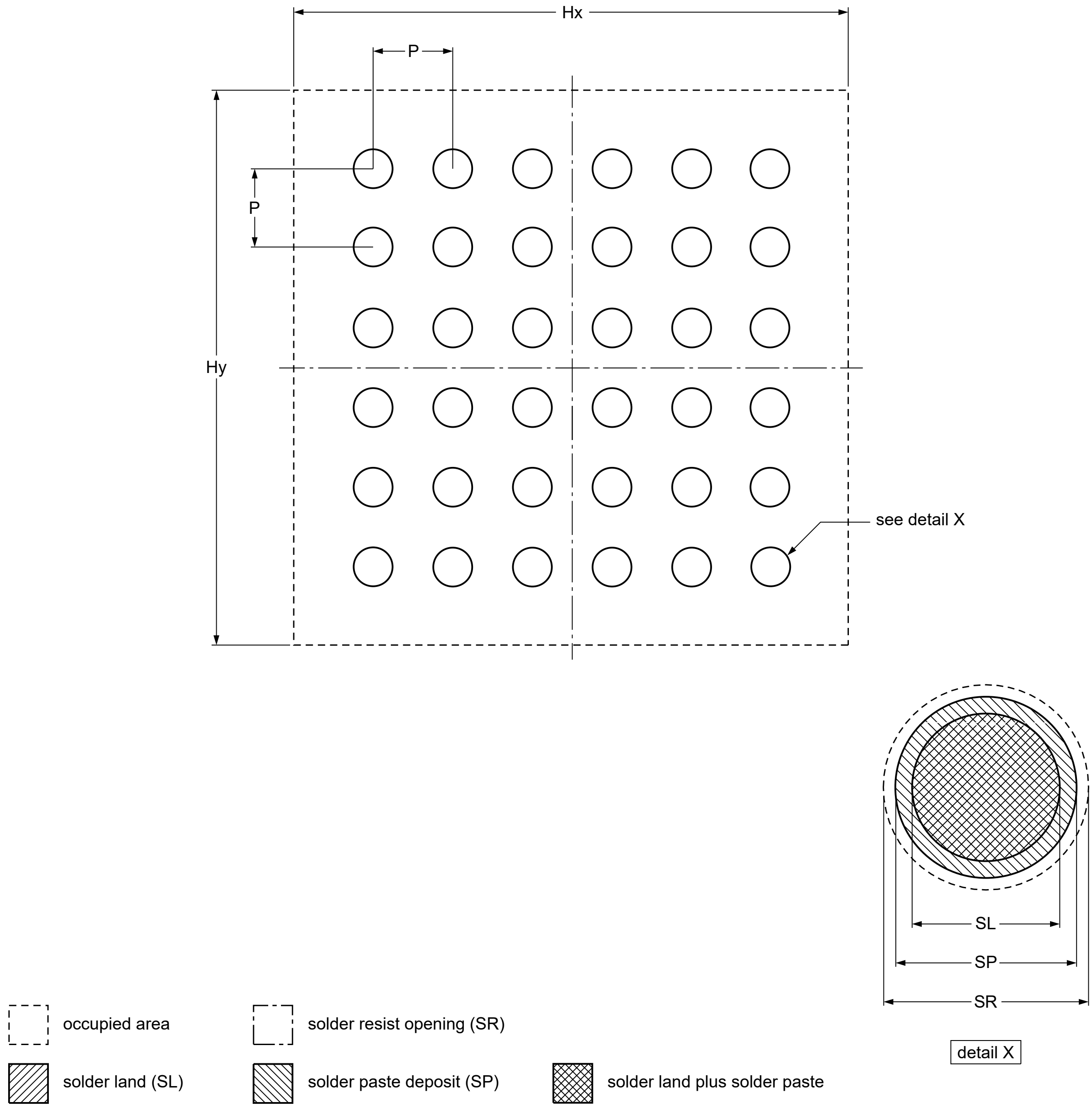
Dimensions in mm Recommended stencil thickness: 0.1 mm

P	Ax	Ay	Bx	By	SLx	SLy	SPx	SPy	SPx tot	SPy tot	C	D	nSPx	nSPy	Gx	Gy	Hx	Hy
0.5	6.0	6.0	4.2	4.2	3.0	3.0	0.7	0.7	1.8	1.8	0.9	0.29	2	2	5.3	5.3	6.25	6.25

Issue date ~~15-06-30~~ 15-07-21 *sot1426-1_fr*

Figure 54. PCB footprint for SOT1426-1 (HUQFN32); reflow soldering

Footprint information for reflow soldering package **SOT1851-1**



Dimensions in mm

recommend stencil thickness: 0.1 mm

P	SL	SP	SR	Hx	Hy
0.40	0.22	0.27	0.30	2.8	2.8

Issue date ~~16-03-30~~ 16-04-13

sot1851-1_fr

Figure 55. PCB footprint for SOT1851-1 (VFBGA36); reflow soldering

18 Acronyms

Table 70 describes the acronyms used in this data sheet.

Table 70. Acronyms

Acronym	Description
ESD	Electrostatic discharge
FET	Field-effect transistor
GPIO	General-purpose input/output
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/output
LED	Light-emitting diode
LSB	Least significant bit
MSB	Most significant bit
NACK	Not Acknowledge
POR	Power-on reset
PRR	Pulse repetition rate
SMBus	System management bus

19 Revision history

Table 71 summarizes revisions to this document.

Table 71. Revision history

Document ID	Release date	Description
PCAL6524 v.2.1	3 July 2025	• Updated per CIN# 202504004I – Table 63: Updated typical value from 34.6 to 42
PCAL6524 v.2	15 May 2019	• Table 2: – Added PCAL6524HEAZ 7"/500u packing option which was inadvertently removed. – Removed PCAL6524DR TSSOP32 package which was removed from the road map.
PCAL6524 v.1.2	24 November 2016	• Added PCAL6524EV • Table 2: Removed PCAL6524HEAZ • Added 0.1 μF bypass capacitor information for $V_{DD(P)}$
PCAL6524 v.1.1	21 September 2016	• Table 61: Updated V_I and V_O
PCAL6524 v.1	22 September 2015	Product data sheet

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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