S32K396

S32K39 and S32K37 Data Sheet

Supports S32K396, S32K394, S32K376 and S32K374.

Rev. 3 — 03/2024

Data Sheet: Technical Data

This document provides electrical specifications for S32K396.

For functional characteristics and the programming model, see S32K396 Reference Manual.

Contents

1 S32K396 product series

The S32K396 product series further extends the highly scalable portfolio of Arm® Cortex®-M7 K3xx MCUs in the automotive industry. It features:

- The Cortex-M7 core at a higher frequency.
- Advanced motor control coprocessors.
- An extended analog, including a high-resolution PWM.

S32K396 is developed to meet the next generation SiC traction inverter requirements and to enable high efficiency, low latency, and system-level BOM cost savings. Because of its versatile architecture, S32K396 is also well suited to address a wide range of xEV applications.

This document represents S32K396 which is the superset device of the S32K39 and S32K37 family. The S32K39x MCUs extend the high-performance capabilities of S32K37x with two programmable motor control coprocessors. The last digit denotes the size of Flash memory size. See the Feature comparison for a detailed overview of the differences between variants. When the S32K396 is referenced in the RM it means the conditions, configurations or features are valid for all the variants of the device.

S32K396 can also be used in combination with powerful 16 nm NXP MCUs or MPUs (S32Z2 and S3E2), in these ways:

- As a companion die: connected locally (same ECU) to S32Z2 and S3E2 through the Zipwire interface to extend 5V I/O and analog capabilities
- As a smart actuator: connected remotely via Ethernet or FlexCAN

2 Block diagrams

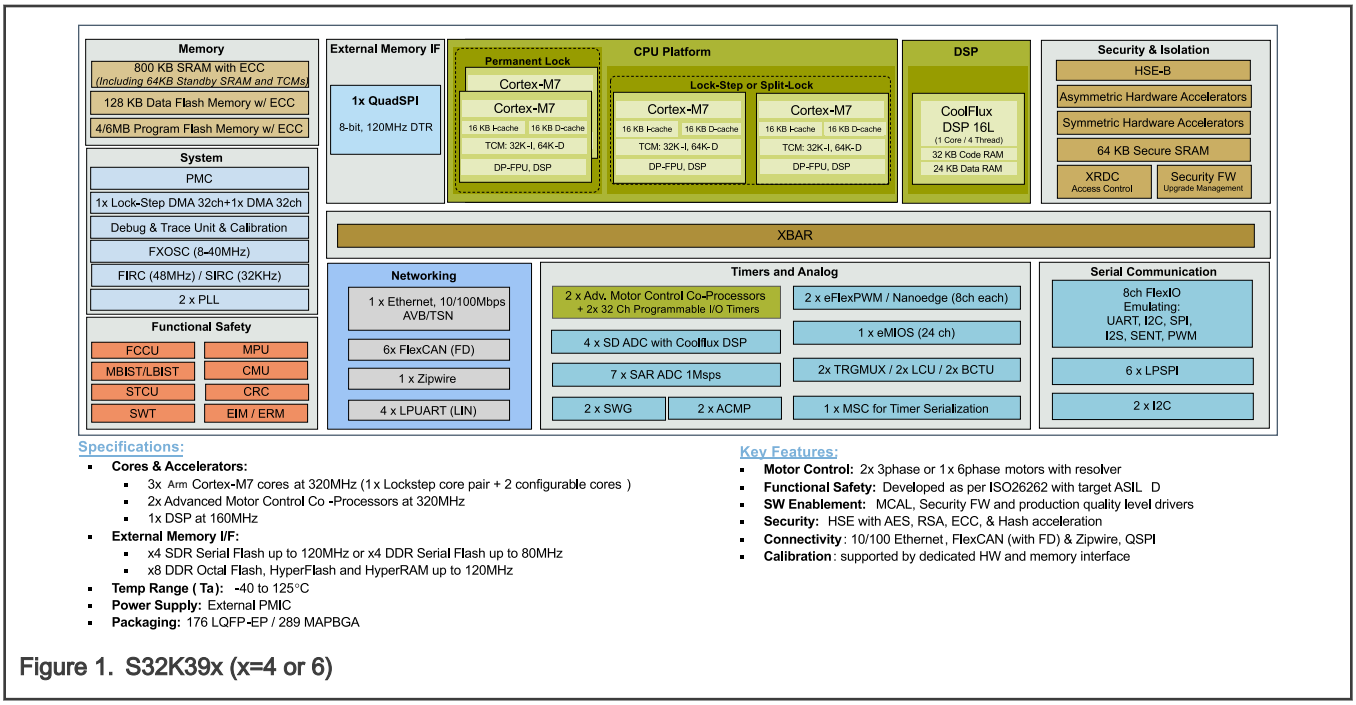
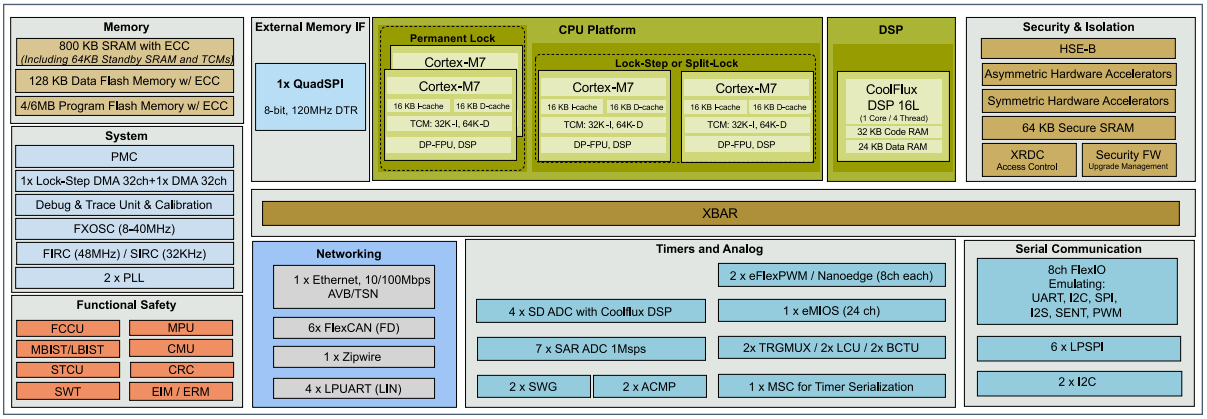


Figure 1. S32K39x (x=4 or 6)



Specifications:

- **Cores & Accelerators:**
  - 3x Arm Cortex-M7 cores at 320MHz (1x Lockstep core pair + 2 configurable cores)
  - 1x DSP at 160MHz
- **External Memory I/F:**
  - x4 SDR Serial Flash up to 120MHz or x4 DDR Serial Flash up to 80MHz
  - x8 DDR Octal Flash, HyperFlash and HyperRAM up to 120MHz
- **Temp Range (Ta):** -40 to 125°C
- **Power Supply:** External PMIC
- **Packaging:** 176 LQFP-EP / 289 MAPBGA

Key Features:

- **Motor Control:** 1x 3phase with resolver
- **Functional Safety:** Developed as per ISO26262 with target ASIL D
- **SW Enablement:** MCAL, Security FW and production quality level drivers
- **Security:** HSE with AES, RSA, ECC, & Hash acceleration
- **Connectivity**: 10/100 Ethernet, FlexCAN (with FD) & Zipwire, QSPI
- **Calibration**: supported by dedicated HW and memory interface

Figure 2. S32K37x (x=4 or 6)

3 Features

3.1 Feature comparison

The following table compares some of the prominent features of the S32K396 product series.

Table 1. Feature comparison

Feature	S32K396	S32K394	S32K376	S32K374
Safety/ASIL	ASIL D			
Number of CPU cores	Three Arm® Cortex®-M7 cores			
Core configurations	One lockstep core pair and Two split-lock configurable cores			
Core frequency (MHz)	320			
Program flash memory (MB)	6	4	6	4
Data flash memory (KB)	128			
Total RAM (KB)	800 (including 64 KB standby RAM and 288 KB TCM)			
Standby RAM (KB)	64			
Security	HSE_B			
DMA	2 x 32-channel eDMA (1 eDMA implemented as a lock-step pair)			
Maximum performance (DMIPS)	2054[1] Mixed ASIL 1 core in lockstep (ASIL D) and 2 cores in split-lock (ASIL B)			
ASIL D (DMIPS)	1369			

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Table 1. Feature comparison (continued)

Feature	S32K396	S32K394	S32K376	S32K374
Advanced motor control coprocessor configuration	2 x eTPU engines at a frequency of 320 MHz (32 channels each) with an input glitch filter		N/A	
DSP (CoolFlux) [MHz]	160			
eFlexPWM configuration	2 x eFlexPWM with NanoEdge (8 channels each)			
FlexCAN instances	6			
EMAC configuration	1 x 10/100 Mbit/s			
LPUART (LIN) instances	4			
Zipwire instances[2]	1			
QuadSPI instances	1			
LPSPI instances	6[3]			
I^2C instances	2			
FlexIO configuration	8 channels, 32 pins Emulating UART, I^2C, SPI, I^2S, single edge nibble transmission (SENT), PWM, and camera interface			
MSC instances[4]	1			
SAR_ADC 1-Msps instances	7			
SDADC instances	4			
SWG instances	2			
LPCMP instances	2			
PIT instances	3			
SWT instances	3			
STM instances	3			
LCU instances	2			
BCTU instances	2			
TRGMUX instances	2			
eMIOS instances	1 (24 channels)			
RTC instances	1			
289-ball MAPBGA included?	Yes			

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Table 1. Feature comparison (continued)

Feature	S32K396	S32K394	S32K376	S32K374
176 LQFP-EP included?	Yes			

1. Cortex-M7 core DMIPS/MHz 2.14-3.23.
2. This feature is available for 289 MAPBGA.
3. You can increase the number of channels by using FlexIO emulation.
4. LVDS and single-ended in 289 MAPBGA; single-ended only in 176 LQFP-EP.

3.2 Feature summary

The following table provides a list of Cortex-M7 core features that the S32K396 product family supports.

Table 2. Feature summary

Feature	Inclusions
Core and architecture	• Cortex-M7 core running up to 320 MHz • Arm core based on the Armv7 architecture and ThumbR-2 ISA • 16 KB data and 16 KB I-cache for optimizing wait state execution from memories • 96 KB TCM associated with each core • On-core MPU for dynamic task protection (16 regions) • IEEE 754-compliant SPFPU • Harvard bus architecture implementing dedicated instruction and data path • 5-stage pipeline with branch speculation • XRDC integrated with a crossbar switch to provide memory and peripheral protection • DSP and SIMD extension • I/O protection (VIRT_WRAPPER) • embedded trace macrocell (ETM) supporting instruction trace • Arm third-party ecosystem support: software and tools to help minimize development time and cost
DSP and coprocessors	• CoolFlux DSP16L with: — A frequency of 160 MHz — One core and four threads — 32 KB Instruction RAM and 24 KB Data RAM • Two coprocessor cores at a frequency of 320 MHz each that help with: — Software running independently of the Cortex-M7 CPUs — 32 KB code RAM and 8 KB data RAM

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Table 2. Feature summary (continued)

Feature	Inclusions
	— DSP and mathematical capabilities • Extra safety features such as ECC, watchdog, latency monitor, and idle counter
DMA	• 2 x 64-channel DMAMUX per eDMA • 2 x 32-channel eDMAs (1 eDMA implemented as a lock-step pair) • Complex data transfers performed with minimal intervention from a host processor • Programmable support for scatter-gather DMA processing
System and power management	• Support for simplified power modes (Run and Standby) • Support for clock gating of unused modules; specific peripherals continue to work in low-power modes • Support for an external ballast transistor to generate core supply • Fully independent CPU and peripheral clocking scheme • Rapid start-up from a 48 MHz FIRC • Low-power oscillator such as the 32 kHz SIRC • PMC with LVD and selectable trip points • Support for multiple power modes • NMI
Memory and memory interfaces	• Up to 6 MB program flash memory with an ECC • Up to 128 KB data flash memory with an ECC • Up to 800 KB SRAM with an ECC • 8-bit QuadSPI • 120 MHz DTR
Clocks	• External 8–40 MHz crystal oscillator or resonator • Internal clock references: — 48 MHz FIRC ± 5% — 32 kHz SIRC ± 10% • Up to 640 MHz PLL for divided system clock operation
Security and integrity	• HSE_B: Upgradable firmware that NXP delivers and you can program • Security ciphers: — Symmetric: AES with 128, 192, or 256 bits — Cipher modes: ECB, CBC, cipher-based message authentication code (CMAC), GMAC, Counter-Based Block Cipher mode

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Table 2. Feature summary (continued)

Feature	Inclusions
	(CTR), Output-Feedback-Based Block Cipher mode (OFB), counter with cipher block chaining message authentication code (CCM), and Galois/Counter mode (GCM) — Asymmetric: RSA (up to 4096 bytes) and ECC (up to 521 bytes) — Hash: Miyaguchi-Preneel, SHA-2/SHA-3 (up to 512 bytes) — Number of keys that the HSE_B firmware configures and controls — Random number generator • Security use cases supported: — OTA update — Secure boot — Secure communication — Component protection — Secure storage — Key exchange
Safety ISO26262	• Classification up to ASIL D • ERM and EIM support • Watchdog timers with an independent clock source • Voltage monitors • Bandgap voltage available as ADC input • External clock source monitoring using an independent reference • PLL lock and loss-of-lock protection • XRDC • Access control, memory protection, and peripheral isolation • ECC on code flash memory, data flash memory, and system RAM • ADC self-test feature • Internal analog monitoring of all supplies available • CRC generation module • FCCU failure output
Analog	• 12-bit ADC: — Up to 69 external analog inputs — 1 µs conversion time — Internal bandgap voltage reference channel, supporting automatic compare and an optional hardware trigger

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Table 2. Feature summary (continued)

Feature	Inclusions
	— Up to five internal reference inputs — Automatic compare with interrupt — Self-test and self-calibration scheme • SDADC: — Integrated digital filtering (CoolFlux DSP) • SGEN (Sine Wave Generator) — Input clock frequency range: 12 MHz–20 MHz — Output sinusoidal signal frequency range: 1 kHz–50 kHz • LPCMP with an internal 8-bit DAC as a reference: — LPCMP with both positive and negative inputs, with separately selectable interrupts on rising and falling comparator outputs — Ability to cross-trigger the timers from both the ADC and LPCMP outputs • Temperature sensor (TempSense) with an output that ADC measures
I/O timers	• eFlexPWM with NanoEdge (high-resolution PWM): — 16 bits (+5 with NanoEdge) of resolution for center-aligned, edge-aligned, and asymmetrical PWMs — Support for double switching PWM outputs — Fault inputs that can be assigned to control multiple PWM outputs — Independent top and bottom hardware deadtime insertion — Multiple output trigger events that can be generated per PWM cycle via hardware • 24-bit eMIOS timer, offering up to 24 standard channels: — Input Capture, Output Compare, and PWM modes — Fault input support with global fault control — Multiple features such as deadtime insertion, configurable polarity, quadrature decoding, and so on • Motor control and power conversion using a combination of eTPU, eFlexPWM, eMIOS, LCU, BCTU, and SWG • 3 x STMs, with four channels each • 32-bit RTC • 3 x 32-bit PITs, with four channels for raising interrupts and triggering DMA channels
Communications	• LPSPI supporting DMA with full-duplex or single-wire bidirectional communication in Master or Slave mode

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Table 2. Feature summary (continued)

Feature	Inclusions
	• LPI2C modules with: — DMA support — Low-power availability — Master or slave support — System management bus • FlexIO, with an option to configure as different communication peripherals, offering support for SENT • LPUART with DMA support, having: — An optional 13-bit break — Full-duplex NRZ — LIN 2.1 extension support — Low-power availability • FlexCAN modules with ISOCAN-FD and DMA support • EMAC complex (10/100 Ethernet) that supports 1588 timers, MII/RMII interface, and AVB and TSN support • Microsecond channel (MSC) • Zipwire (high-speed SIPI and LFAST)
Debug	• Debug watchpoint and trace (DWT), with four configurable comparators as hardware watch points • SWO-synchronous trace data support • Instrumentation trace macrocell (ITM) with software and hardware trace plus timestamping • FPB with an ability to patch code and data from code space to system space • All execution units and bus masters made traceable through TPIU over GPIO pins; a very-low-bandwidth trace option also available via the SWO • embedded trace FIFO (ETF): a dedicated trace buffer available for each of the core masters, allowing data to be captured internally before being optionally routed to external trace pins • Serial wire viewer (SWV): trace capability providing displays of: — Reads — Writes — Exceptions — PC samples — Print

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Table 2. Feature summary (continued)

Feature	Inclusions
I/O and package	• Up to 237 GPIO pins • Up to 144 GPIO pins with interrupt functionality • Up to 77 GPIO pins with wakeup capability • Pseudo open-drain support on LPUART, FlexIO, and LPI2C • Package options of 289 MAPBGA and 176 LQFP-EP

4 Ordering information

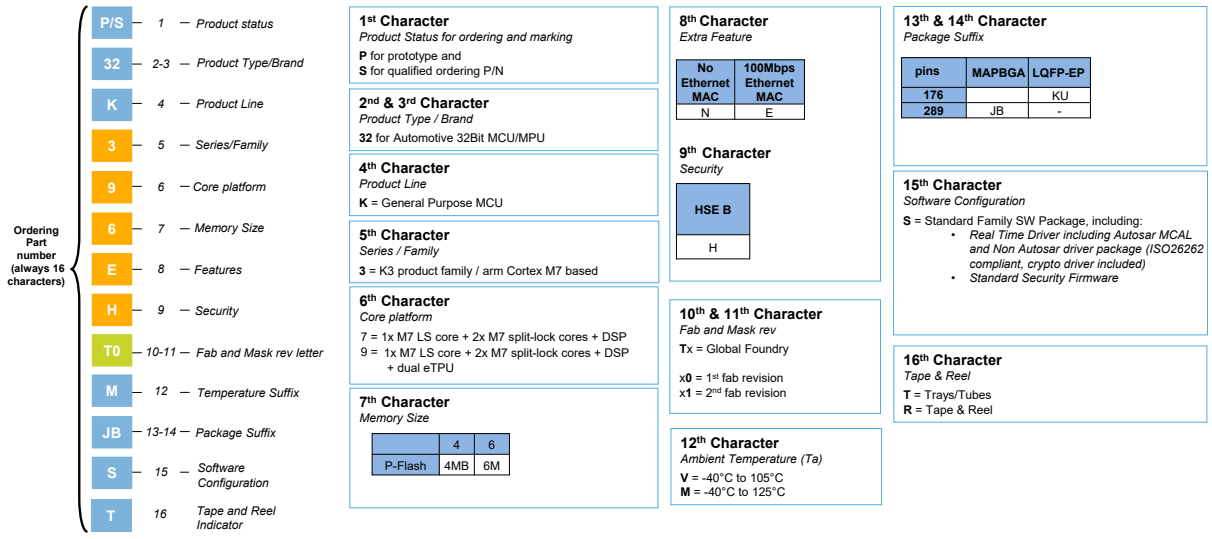

Figure 3. Ordering information

5 General

5.1 Absolute maximum ratings

CAUTION

When the MCU is in an unpowered state, current injected through the chip pins may bias internal chip structures (for example, ESD diodes) and incorrectly power up these internal structures through inadvertent paths. The presence of such residual voltage may influence different chip-internal blocks in an unpredictable manner and may ultimately result in unpredictable chip behavior (for example, POR flag not set). Once in the illegal state, powering up the chip further and then applying reset will clear the illegal state. Injection current specified for the chip under the aspect of absolute maximum ratings represent the capability of the internal circuitry to withstand such condition without causing physical damage. Functional operation of the chip under conditions - specified as absolute maximum ratings - is not implied.

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in the following table for specific conditions. Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device. All the limits defined in the datasheet specification must be honored together and any violation to any one or more will not guarantee desired operation. Unless otherwise specified, all maximum and minimum values in the datasheet are across process, voltage, and temperature.

Table 3. Absolute maximum ratings

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_HV_A	Main I/O and analog supply voltage [1,2]	-0.3	—	6.0	V	—	—
VDD_HV_B	Secondary I/O supply voltage [1,2]	-0.3	—	6.0	V	—	—
VDD_DCDC	Supply voltage for the SMPS gate driver [1,2,3]	-0.3	—	6.0	V	—	—
V15	Voltage sensing input [1,2]	-0.3	—	2.75	V	—	—
V25	Flash memory supply (2.5 V), internally regulated [1]	-0.3	—	2.9	V	—	—
V11	High-current core logic supply input [1]	-0.3	—	1.26	V	—	—
VDDA_SWG	Supply voltage for SWG [1,2]	-0.3	—	6.0	V	—	—
VDD_LVDS	Supply voltage for LVDS [1,2]	-0.3	—	3.96	V	—	—
VREFH_ADC_0123, VREFH_ADC_456	ADC high reference voltage [1,2]	-0.3	—	6.0	V	—	—
VREFL_ADC_0123, VREFL_ADC_456	ADC low reference voltage [1]	-0.3	—	0.3	V	—	—
VREFH_SDADC_01, VREFH_SDADC_23	SDADC high reference voltage [1,2]	-0.3	—	6.0	V	—	—
VREFL_SDADC_01, VREFL_SDADC_23	SDADC low reference voltage [1]	-0.3	—	0.3	V	—	—
VGPIO_trans	Transient overshoot voltage	-	—	6.0	V	—	—

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Table 3. Absolute maximum ratings (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	allowed on I/O pin [1,2,4]						
I_INJPAD_DC_ABS	Continuous DC input current (positive/negative) that can be injected into an I/O pin [5]	-3	—	3	mA	—	—
I_INJSUM_DC_ABS	Sum of absolute value of injected currents on all the I/O pins (continuous DC limit) [5]	—	—	30	mA	—	—
TSTG	Storage ambient temperature [6]	-55	—	150	°C	—	—

1. All voltages are referred to VSS unless otherwise specified.
2. 6.0 V maximum for 10 hours over lifetime; 7.0 V maximum for 60 seconds over lifetime.
3. Voltage at VDD_DCDC cannot be higher than VDD_HV_A.
4. Absolute max rating must be honored under all conditions, including current injection.
5. When input pad voltage levels are close to VDD_HV_A (respectively to VDD_HV_B) or VSS, practically no current injection is possible. See application note AN4731 for a description of injection current on NXP automotive microcontrollers.
6. TSTG specifies the storage temperature range. It is not the operating temperature range. Please refer to the Thermal operating characteristics table.

5.2 Voltage and current operating requirements

NOTE

Device functionality is guaranteed down to the LVR assert level, however electrical performance of 12-bit ADC, CMP with 8-bit DAC, IO electrical characteristics, and communication modules electrical characteristics will be degraded when voltage drops below 2.97 V.

NOTE

DSPI/MSC interface is supported only at VDD_HV_A = 5V.

Table 4. Voltage and current operating requirements

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_HV_A	Main I/O and analog supply voltage [1]	2.97	3.3 or 5.0	5.5	V	—	—
VDD_HV_B	Secondary I/O supply voltage [1]	2.97	3.3 or 5.0	5.5	V	—	—
VDD_DCDC	Supply voltage for the SMPS gate driver [1,2]	2.97	3.3 or 5.0	5.5	V	—	—

Table continues on the next page...

Table 4. Voltage and current operating requirements (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
V15	Voltage sensing input [1,3]	1.425	1.5	1.65	V	—	—
VDDA_SWG	Supply voltage for SWG [1,4]	2.97	3.3 or 5.0	5.5	V	—	—
VDD_LVDS	Supply voltage for LVDS [1,5]	2.97	3.3	3.63	V	—	—
VDD_SDADC	Supply voltage for SDADC [1,4,6]	4.5	5	5.5	V	—	—
VREFH_SAR_0123, VREFH_SAR_456	SAR ADC high reference voltage [1,7,8]	2.97	3.3 or 5.0	5.5	V	—	—
VREFL_SAR_0123, VREFL_SAR_456	SAR ADC low reference voltage [1]	-0.1	0	0.1	V	—	—
VREFH_SDADC_01, VREFH_SDADC_23	SDADC high reference voltage [1,6,7,8]	4.5	5.0	5.5	V	—	—
VREFL_SDADC_01, VREFL_SDADC_23	SDADC low reference voltage [1]	-0.1	0	0.1	V	—	—
VREFH_R2R	R2R high reference voltage [8]	4.5	5.0	5.5	V	—	—
VREFL_R2R	R2R low reference voltage	-0.1	0	0.1	V	—	—
VSS_DCDC	Power ground for the SMPS gate driver [1]	-0.1	0	0.1	V	—	—
V25	Flash memory and clock supply (2.5 V), internally regulated [1]	—	2.5	—	V	—	—
V11	High-current core logic supply input [1]	—	1.14	—	V	—	—
VGPIO	Input voltage range at any I/O or analog pin [1]	-0.3	—	VDD_HV_A/B + 0.3	V	—	—
VODPU	Open-drain pull-up voltage [1,9]	—	—	VDD_HV_A/B	V	—	—
IINJPAD_DC_OP	Continuous DC input current (positive/ negative) that can be	-3	—	3	mA	VDD_HV_A >= 3.6V	—

Table continues on the next page...

Table 4. Voltage and current operating requirements (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	injected into an I/O pin [10]						
IINJPAD_DC_OP	Continuous DC input current (positive/ negative) that can be injected into an I/O pin [10]	-2	—	3	mA	VDD_HV_A >= 2.97V	—
IINJSUM_DC_OP	Sum of absolute value of injected currents on all the I/O pins (continuous DC limit) [10]	-30	—	30	mA	VDD_HV_A >= 3.6V	—
IINJSUM_DC_OP	Sum of absolute value of injected currents on all the I/O pins (continuous DC limit) [10]	-20	—	30	mA	VDD_HV_A >= 2.97V	—
IINJ_LVDS	Max LVDS RX or TX pin injection current	0	—	100	µA	—	—
Vramp_slow	Supply ramp rate (slow) [1,11]	0.5	—	—	V/min	—	—
Vramp_fast	Supply ramp rate (fast) [1,11]	—	—	100	V/ms	—	—

1. All voltages are referred to VSS unless otherwise specified.
2. Voltage at VDD_DCDC cannot be higher than VDD_HV_A
3. Min and Max values are applicable only for non-SMPS mode where V15 is sourced externally.
4. Must be shorted to VDD_HV_A at the PCB level
5. Ensure that VDD_HV_A ramps before VDD_LVDS.
6. SDADC is intended to be used only when VDD_HV_A is supplied with 5V. In case of VDD_HV_A is supplied with 3.3V it is recommended to disable SDADC in MC_ME module
7. VREFH should always be equal to or less than VDD_HV_A +0.1. Any positive differential voltage between VREFH and VDD_HV_A i.e., VDD_HV_A < VREFH <= VDD_HV_A + 0.1V) is for RF-AC only. Appropriate decoupling capacitors should be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC
8. All the VREFH_xx except of VREFH_R2R must be shorted to single supply source at the PCB level, either isolated voltage reference or shorted to VDD_HV_A. Isolated VREFH_R2R is required to avoid SDADC performance degradation. If isolated supply cannot be used, then appropriate filtration is needed to isolate the VREFH_R2R noise
9. Open-drain outputs must be pulled respectively to their supply rail (VDD_HV_A or VDD_HV_B).
10. When input pad voltage levels are close to VDD_HV_A (respectively to VDD_HV_B) or VSS, practically no current injection is possible.
11. The MCU supply ramp rate parameter must be applicable to the MCU input/external supplies. The ramp rate assumes that the S32K396 Hardware design guidelines document available on http://www.nxp.comare followed.

If total power dissipation and maximum junction temperature allows. Please refer to Thermal operating characteristics table for the maximum junction temperature, and Thermal characteristics table for the thermal characteristics, to determine the maximum power dissipation allowed for a given package.

Voltage at VDD_DCDC cannot be higher than VDD_HV_A.

5.2.1 Supported voltage supply use-cases

Table 5. Supported voltage supply use-cases

	VDD_HV_A is 3.3 V	VDD_HV_A is 5 V
VDD_HV_B is 3.3 V	yes	yes
VDD_HV_B is 5 V	no	yes

5.3 Thermal operating characteristics

Table 6. Thermal operating characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Tamb	Ambient temperature	-40	—	125	°C	—	—
TJ	Junction temperature	-40	—	150	°C	—	—

5.4 ESD and Latch-up Protection Characteristics

Table 7. ESD and Latch-up Protection Characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Vhbm	Electrostatic discharge voltage, human body model (HBM) [1,2,3]	-2000	—	2000	V	—	—
Vcdm	Electrostatic discharge voltage, charged-device model (CDM), all pins except corner [1,3,4]	-500	—	500	V	—	—
Vcdm	Electrostatic discharge voltage, charged-device model (CDM), corner pins [1,3,4]	-750	—	750	V	—	—
Ilat	Latch-up current at ambient temperature of 125°C [5]	-100	—	100	mA	—	—

1. Device failure is defined as: "If after exposure to ESD pulses, the device does not meet specification requirements."
2. This parameter is tested in conformity with AEC-Q100-002.
3. All ESD testing conforms with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
4. This parameter is tested in conformity with AEC-Q100-011.
5. This parameter is tested in conformity with AEC-Q100-004.

6 Power management

6.1 Supply Monitoring

Table 8. Supply Monitoring

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
HVD_V15	High Voltage Detect (HVD) on V15, assert threshold (in FPM) [1]	—	2.5	—	V	—	—
LVR_VDD_HV_A	LVR on VDD_HV_A, assert threshold (in FPM)	2.77	2.85	2.93	V	—	—
LVR_VDD_HV_A	LVR on VDD_HV_A, assert threshold (in RPM)	2.77	2.85	2.93	V	—	—
—	VDD_HV_A LVR monitor hysteresis	—	18.75	—	mV	—	—
HVD_VDD_HV_A	HVD on VDD_HV_A, assert threshold (in FPM)	5.787	5.887	5.987	V	—	—
—	VDD_HV_A HVD monitor hysteresis	—	37.5	—	mV	—	—
LVR_VDD_HV_B	LVR on VDD_HV_B, assert threshold (in FPM)	2.77	2.85	2.93	V	—	—
LVR_VDD_HV_B	LVR on VDD_HV_B, assert threshold (in RPM)	2.77	2.85	2.93	V	—	—
—	VDD_HV_B LVR monitor hysteresis	—	18.75	—	mV	—	—
HVD_VDD_HV_B	HVD on VDD_HV_B, assert threshold (in FPM)	5.787	5.887	5.987	V	—	—
—	VDD_HV_B HVD monitor hysteresis	—	37.5	—	mV	—	—
LVD_VDD_LVDS	LVD on VDD_LVDS, assert threshold (in FPM)	2.77	2.85	2.93	V	—	—
—	VDD_LVDS LVD monitor hysteresis	—	18.75	—	mV	—	—
LVD_VDD_HV_A	Low Voltage Detect (LVD5A) on	4.33	4.41	4.49	V	—	—

Table continues on the next page...

Table 8. Supply Monitoring (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	VDD_HV_A, assert threshold (in FPM)						
—	VDD_HV_A LVD monitor hysteresis	—	37.5	—	mV	—	—
VPOR_VDD_HV_A	Power-On-Reset (VPOR) on VDD_HV_A, deassert threshold	0.9	1.5	2.2	V	—	—
VREF12	Bandgap reference, trimmed	1.18	1.2	1.22	V	—	—

1. The HVD_V15 monitor is provided to indicate if the V15 rail is far above the standard V15 operating range , to ensure failures in the V15 regulator are detected

6.2 Recommended Decoupling Capacitors

Table 9. Recommended Decoupling Capacitors

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
CDEC	Decoupling capacitor (one per supply pin, at least one per side) [1,2,3]	70	100	—	nF	—	—
CBULK	Input supply bulk capacitor [3,4,5,6]	—	4.7	—	µF	—	—
COUT_V11	V11 (1.1V Regulator) output capacitor [3]	—	22	—	µF	—	—
COUT_V25	V25 (2.5V Regulator) output capacitor [2,3]	140	220	—	nF	—	—

1. Optionally, 10 nF capacitors can be added in parallel to the decoupling capacitors.
2. These capacitors must be placed as close as possible to the corresponding supply and ground pins. For BGA packages, the capacitors must be placed on the other side of the PCB to minimize the trace lengths.
3. All capacitors must be low ESR ceramic capacitors (for example, X7R). The minimum recommendation is after considering component aging and tolerance.
4. For devices where the VDD_HV_B domain is present, if the VDD_HV_B supply is different supply from VDD_HV_A, a dedicated bulk capacitor is needed.
5. It is also possible to use higher capacitance values (for example, 10 µF) in place of the 4.7 µF capacitor.
6. These capacitors must be placed close to the source.

Only needed when internal SMPS is used to generate V15 and VDD_DCDC is supplied with isolated source from VDD_HV_A or VDD_HV_B

For devices where V15 is present, the V15 regulator output capacitor and the filter capacitors are required when using an NPN bipolar ballast transistor for the regulation stage. When V15 is supplied from an external regulator, these capacitance recommendations can be followed in addition to the capacitance requirements of the external voltage regulator.

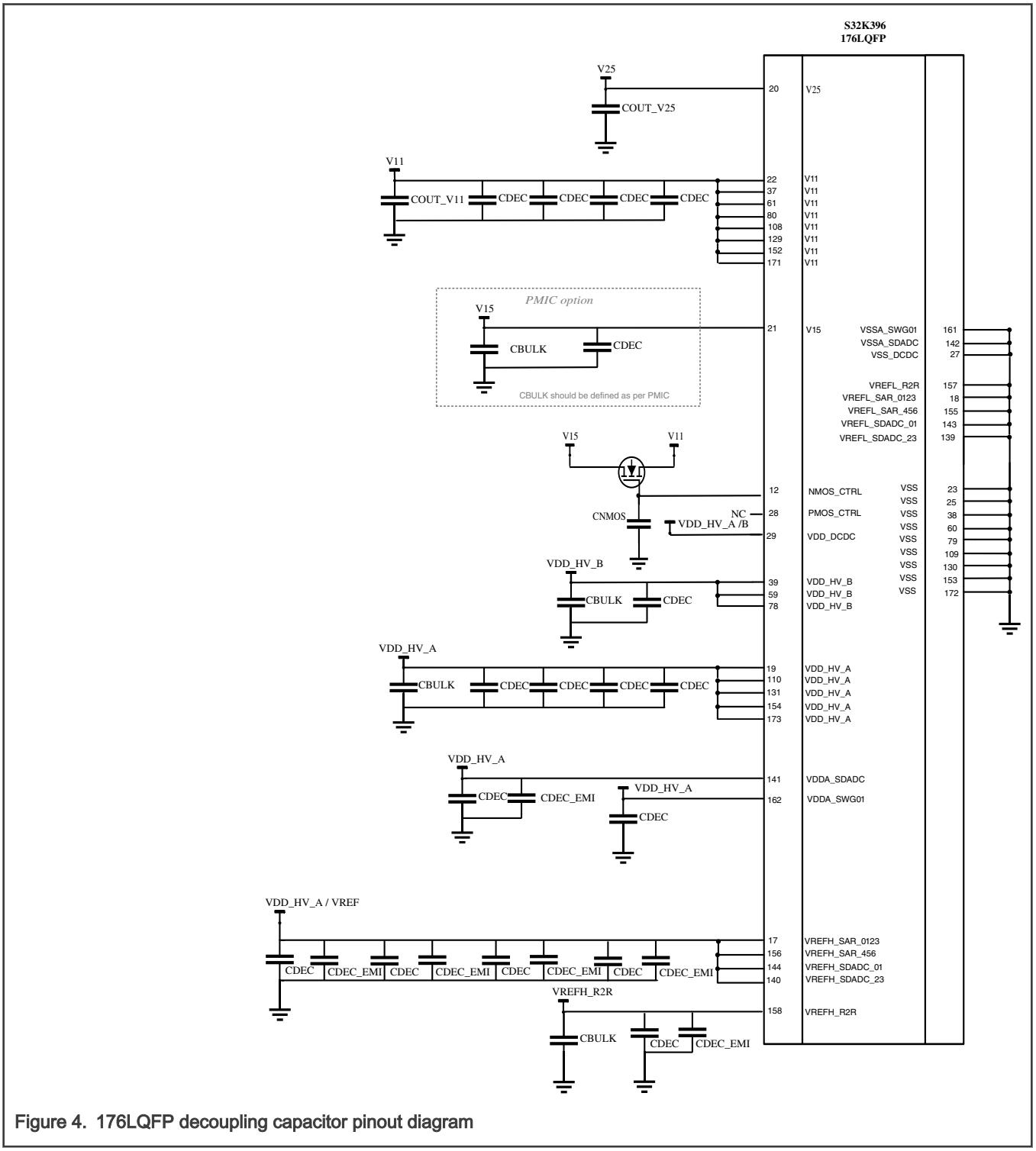

Figure 4. 176LQFP decoupling capacitor pinout diagram

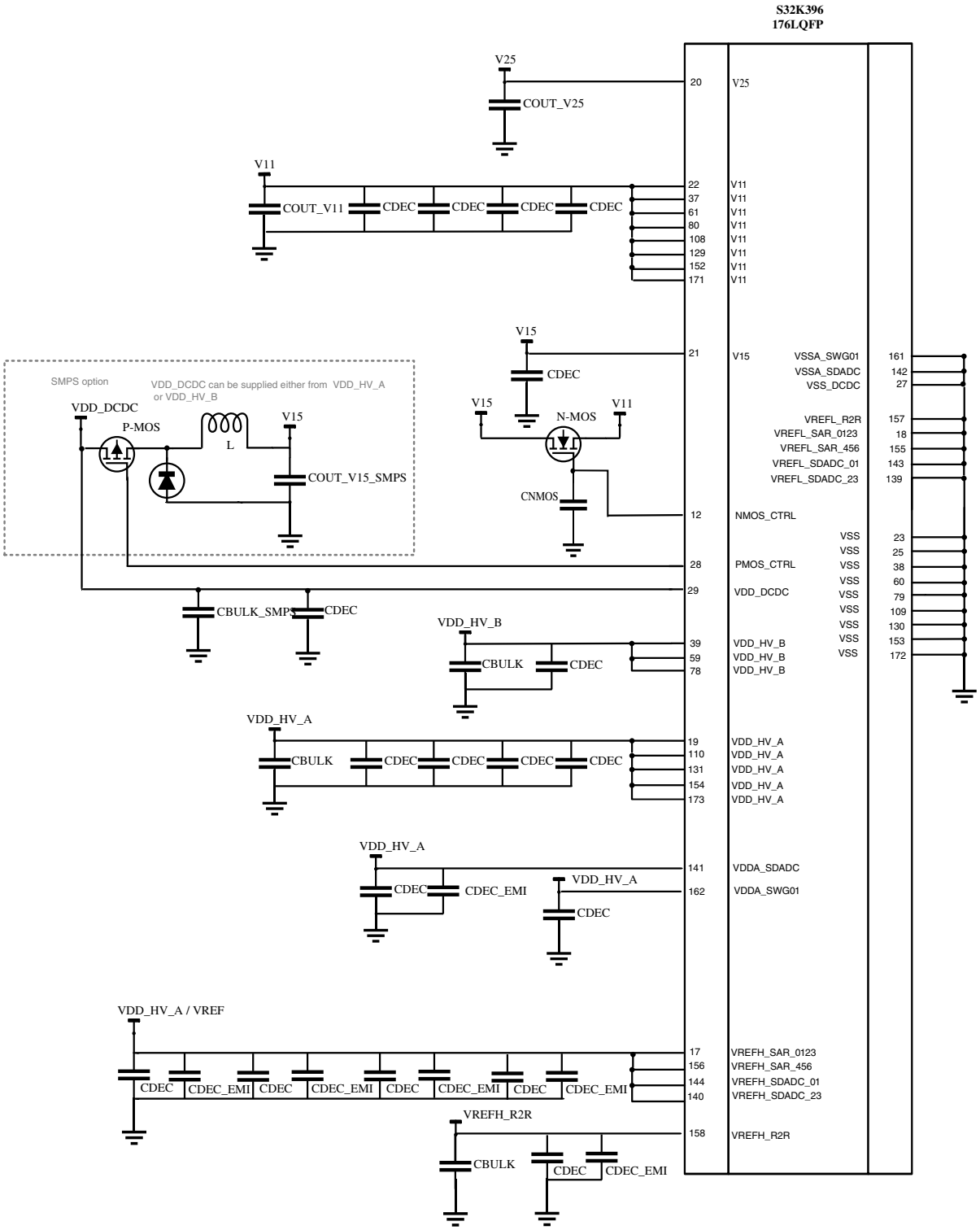

Figure 5. 176LQFP decoupling capacitor pinout diagram (SMPS)

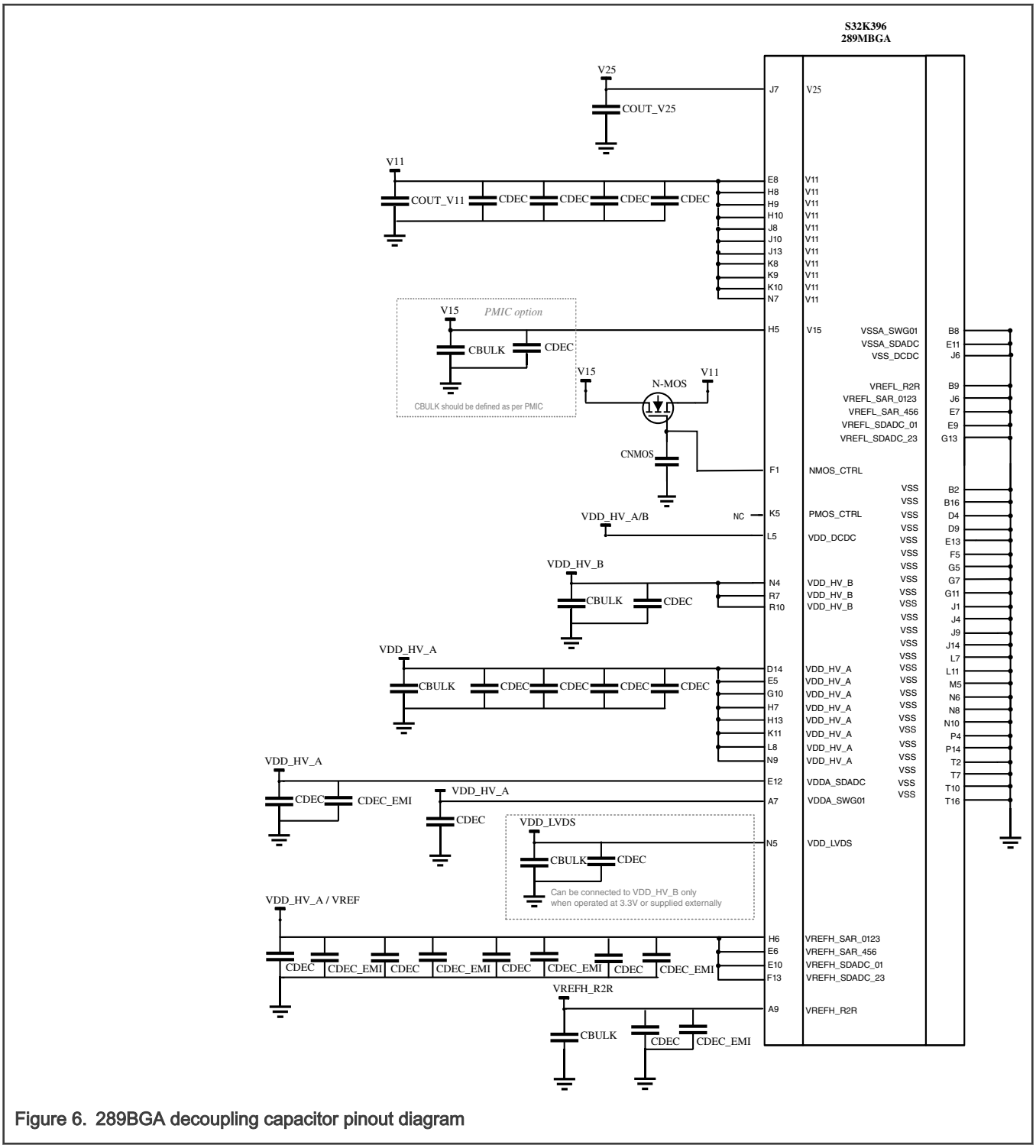

Figure 6. 289BGA decoupling capacitor pinout diagram

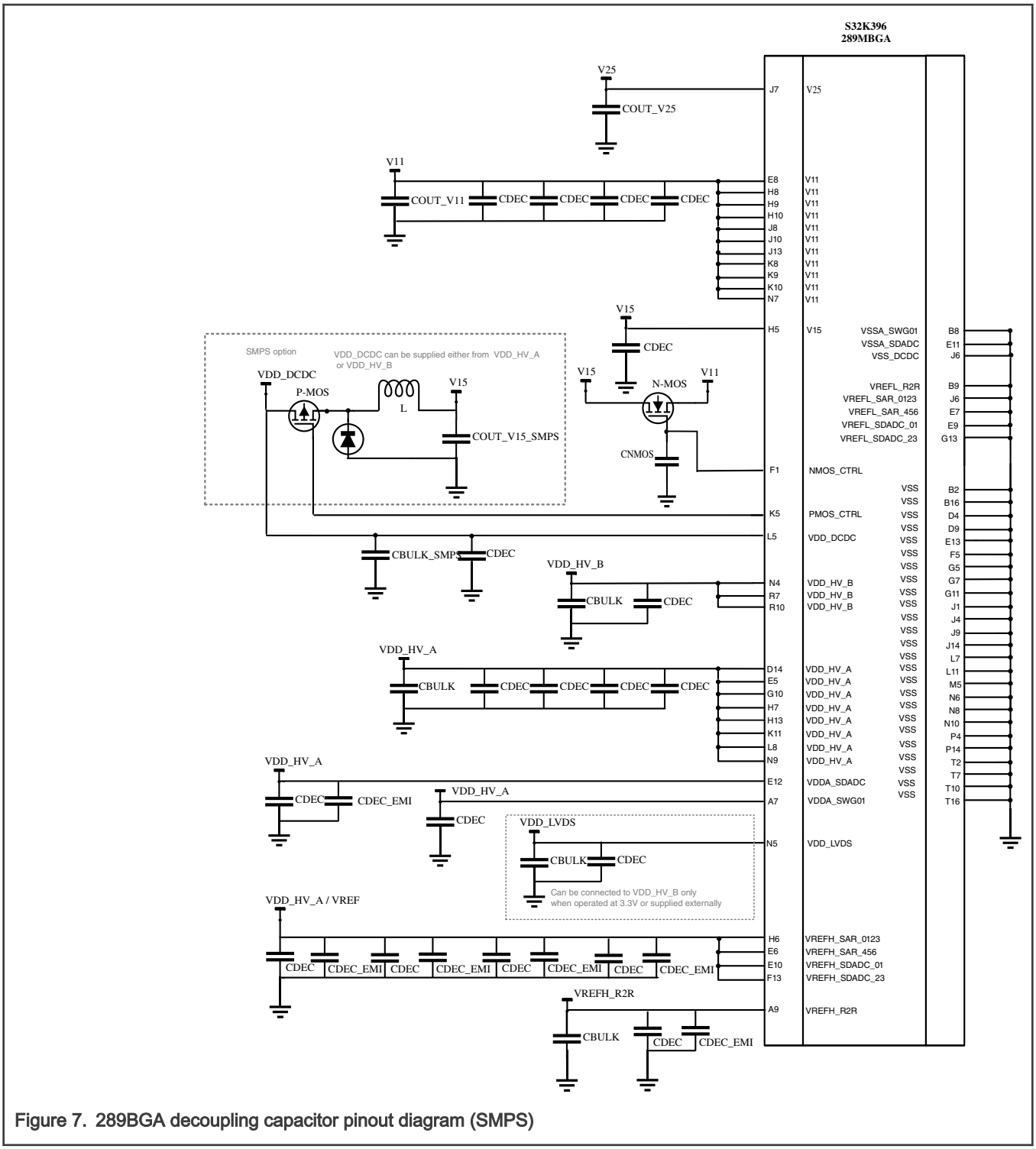

Figure 7. 289BGA decoupling capacitor pinout diagram (SMPS)

6.3 V15 regulator (SMPS option) electrical specifications

The chip hardware design guidelines document lists the recommended part numbers for PMOS, Schottky diode and inductor.

Table 10. V15 regulator (SMPS option) electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
V15	V15 output	—	1.5	—	V	—	—
L_SMPS	External coil inductance	—	4.7	—	uH	—	—
COUT_V15_SMPS	External bypass capacitor	—	20-22	—	uF	—	—
—	External bypass capacitor	—	40-44	—	uF	—	—
D_SMPS	External Schottky diode average forward current	—	2	—	A	—	—
VR	Schottky diode reverse voltage	5.0	—	—	V	—	—
IF	Schottky diode forward current	1.0	—	—	A	—	—
—	External P-channel MOSFET total gate charge	—	—	10	nC	VDD_DCDC = 5V	—
—	External P-channel MOSFET threshold voltage	—	—	2	V	—	—
CBULK_SMPS	Input supply bulk capacitor for internal SMPS [1]	—	22	—	µF	—	—

1. Only needed when internal SMPS is used to generate V15 and VDD_DCDC is supplied with isolated source from VDD_HV_A or VDD_HV_B.

6.4 V11 regulator (NMOS ballast transistor control) electrical specifications

The chip hardware design guidelines document lists the recommended part number for NMOS.

Table 11. V11 regulator (NMOS ballast transistor control) electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
V11	V11 output	—	1.14	—	V	—	—
V15	V15 input	—	1.5	—	V	—	—
VTH_NMOS	Vth of external NMOS	—	—	1.5	V	For 3.3 V supply	—
VTH_NMOS	Vth of external NMOS	—	—	2	V	For 5.0 V supply	—

Table continues on the next page...

Table 11. V11 regulator (NMOS ballast transistor control) electrical specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IDS_NMOS	IDS of external NMOS	3	—	—	A	—	—
tsettle_lm	Required setting time from V11 in FPM to load change	10	—	—	us	—	—
CNMOS	NMOS gate stability capacitor	—	1	—	nF	—	—

6.5 Supply currents

NOTE

All data in this table is preliminary and based on first samples.

Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes VDD_HV_A = VREFH = 5 V, VDD_HV_B = 5V (if the VDD_HV_B domain present in the device), temperature = 25 °C, and typical silicon process unless otherwise stated. In STANDBY configuration, no current flows through the V15 supply.

Table 12. STANDBY mode supply currents

		STANDBY [1]			
		All clocks & peripherals OFF (µA)	SIRC ON (µA)	FIRC ON (24 MHz) (µA)	All Configurations (µA)
Chip	Ambient Temperature (°C)	VDD_HV_A [2]	VDD_HV_A [2]	VDD_HV_A [2]	VDD_HV_B [2]
S32K396, S32K394, S32K376, S32K374	25, typ [3]	75	78	1500	3
	25, max [4]	153	156	1693	3.8
	105, typ [3]	458	461	1869	16
	105, max [4]	1693	1721	3143	62
	125, typ [3]	756	759	2160	27
	125, max [4]	3034	3087	4490	108

1. See the configurations in Table 15.
2. IO load current is not included. The actual current requirements for IOs will depend on the I/O configuration in the application.
3. “typ” is indicative of the average current numbers at the nominal internally regulated V11 supply voltage, VDD_HV_A = 5.0V, VDD_HV_B = 5.0V, for the typical silicon process..

4. “max” is indicative of the maximum current numbers at the maximum internally regulated V11 supply voltage (1.16 V), VDD_HV_A = 5.5V, VDD_HV_B = 5.5V, for the fast silicon process.

NOTE

All data in this table is preliminary and based on first samples.

Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes VDD_HV_A = VREFH = 5 V, temperature = 25 °C, and typical silicon process unless otherwise stated.

Table 13. Low speed RUN mode supply currents

Chip	Ambient Temperature (°C)	Low Speed RUN Mode (mA) [1]				
		BOOT Mode [2] [Clock Option C] FIRC @ 24 MHz		Low Speed RUN [2] [Clock Option D] FIRC @48 MHz		All Configurations [2].
		VDD_HV_A [3, 4]	V11 [5]	VDD_HV_A [3, 4]	V11 [5]	VDD_HV_B [3]
S32K396, S32K394, S32K376, S32K374	25, typ [6]	3.2	61	3.2	93	1.8
	25, max [7]	3.7	156	3.8	188	2.4
	105, typ [6]	3.3	215	3.3	244	1.6
	105, max [7]	4.3	760	4.3	790	2.0
	125, typ [6]	3.4	299	3.4	330	1.5
	125, max [7, 8]	5.3	1105	5.4	1127	2.0

1. Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
2. See the example configurations in Table 15.
3. IO load current is not included. The actual current requirements for IOs will depend on the I/O configuration in the application.
4. RUN IDD @ VDD_HV_A includes Flash memory read current from the V25 voltage rail.
5. V11 is generated by V15 using external NMOS.
6. “typ” is indicative of the average current numbers at the nominal internally regulated V11 supply voltage, VDD_HV_A = 5.0V, VDD_HV_B = 5.0V, V15 = 1.5V, for the typical silicon process.
7. “max” is indicative of the maximum current numbers at the maximum internally regulated V11 supply voltage (1.16 V), VDD_HV_A = 5.5V, VDD_HV_B = 5.5V, V15 = 1.65V, for the fast silicon process.
8. For the maximum allowable RUN current in an application, the junction temperature must be kept below the maximum specification, T_J < 150°C, to avoid self-heating.

NOTE

All data in this table is preliminary and based on first samples.

Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes VDD_HV_A = VDD_HV_B = VREFH = 5 V, temperature = 25 °C and typical silicon process unless otherwise stated.

NOTE

The data in this table is preliminary and based on first samples.

Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes VDD_HV_A VDD_HV_B = VREFH = 5 V, temperature = 25 °C and typical silicon process unless otherwise stated.

Table 14. Example RUN mode configuration supply currents

Chip		RUN Mode (mA) [1]		
	Configurations	2x 3ph Inverters + Resolver eTPU Control (mA) [2] [3]		
	Ambient Temperature (°C)	VDD_HV_A [4] [5]	VDD_HV_B [4]	V11 [6]
S32K396, S32K394, S32K376, S32K374	25, typ [7]	6.4	5.3	547
	25, max [8]	8.7	6.8	654
	105, typ [7]	6.2	5.0	695
	105, max [8]	9.4	6.6	1224
	125, typ [7]	6.3	4.4	777
	125, max [8] [9]	10.2	6.2	1470

1. Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
2. See the configurations in Table 15.
3. VDD_HV_A current will increase/decrease with analog modules as per the use case.
4. IO current is not included. The actual current requirements for IOs will depend on the I/O configuration in the application.
5. RUN IDD @ VDD_HV_A includes Flash memory read current from the V25 voltage rail.
6. V11 is generated by V15 using external NMOS.
7. “typ” is indicative of the average current numbers at the nominal internally regulated V11 supply voltage, VDD_HV_A = 5.0V, VDD_HV_B = 5.0V, V15 = 1.5V, for the typical silicon process.
8. “max” is indicative of the maximum current numbers at the maximum internally regulated V11 supply voltage (1.16 V), VDD_HV_A = 5.5V, VDD_HV_B = 5.5V, V15 = 1.65V, for the fast silicon process.
9. For the maximum allowable RUN current in an application, the junction temperature must be kept below the maximum specification, T_J < 150°C, to avoid self-heating.

6.6 Operating mode

Table 15. STANDBY and low speed RUN configuration options

MODULE	STANDBY All OFF	STANDBY SIRC ON	STANDBY FIRC ON	BOOT Mode (OptionC [1], FIRC @24 MHz)	FIRC Mode (OptionD [1], FIRC @48 MHz)
Core M7_0	OFF	OFF	OFF	OFF	OFF
Core M7_1	OFF	OFF	OFF	OFF	OFF
Core M7_2/3	OFF	OFF	OFF	24 MHz	Limited Activity
HSE_B	OFF	OFF	OFF	OFF	OFF
FIRC	OFF	OFF	24 MHz	24 MHz	48 MHz
FXOSC	OFF	OFF	OFF	OFF	OFF
SIRC	OFF	ON	OFF	ON	ON
PLL	OFF	OFF	OFF	OFF	OFF
Flash	OFF	OFF	OFF	ON	ON
eDMA	All OFF	All OFF	All OFF	All OFF	All OFF
FlexCAN	All OFF	All OFF	All OFF	All OFF	All OFF
LPUART	All OFF	All OFF	All OFF	All OFF	All OFF
LPSPI	All OFF	All OFF	All OFF	All OFF	All OFF
LPI2C	All OFF	All OFF	All OFF	All OFF	All OFF
EMAC	OFF	OFF	OFF	OFF	OFF
Zipwire	OFF	OFF	OFF	OFF	OFF
eMIOS	All OFF	All OFF	All OFF	All OFF	All OFF
eTPU	All OFF	All OFF	All OFF	All OFF	All OFF
eFlexPWM	All OFF	All OFF	All OFF	All OFF	All OFF
IGF	All OFF	All OFF	All OFF	All OFF	All OFF
SD_ADC	All OFF	All OFF	All OFF	All OFF	All OFF
SWG	All OFF	All OFF	All OFF	All OFF	All OFF
SAR_ADC	All OFF	All OFF	All OFF	All OFF	All OFF

Table continues on the next page...

Table 15. STANDBY and low speed RUN configuration options (continued)

MODULE	STANDBY All OFF	STANDBY SIRC ON	STANDBY FIRC ON	BOOT Mode (OptionC [1], FIRC @24 MHz)	FIRC Mode (OptionD [1], FIRC @48 MHz)
LPCMP	All OFF	All OFF	All OFF	All OFF	All OFF

1. See clocking use case examples in the Clocking chapter of the S32K396 Reference Manual.

Table 16. RUN mode configuration options

Config		Inverter Use-cases (Standalone or Smart Actuator)
		2x 3ph Inverters + Resolver eTPU Control
		K39x
Ambient Temperature		125C
CORE & PLATFORM	CM7_0	320MHz
	CM7_1	320MHz
	CM7_2/3 (LS)	320MHz
	Code Caches	ON
	Data Caches	OFF
	eDMA	2
	HSE [1]	80MHz (WFI)
TIMERS	eTPUA	320MHz
	eTPUB	320MHz
	eFlexPWM[2]	12 CH
	eMIOS [3]	6 CH
	Microsecond Channel(MSC)	OFF
ANALOG	1Msps SAR-ADC [4]	7 CH
	SD-ADC + Coolflux	4 CH
	SWG	2
COMMS	Zipwire	OFF
	Ethernet	ON
	CAN-FD	4
	SPI	5
	LIN	OFF
	I2C	2
MEMORY	QuadSPI	OFF

Table continues on the next page...

Table 16. RUN mode configuration options (continued)

	Flash Size	4M and 6M
TARGET PACKAGE	176 LQFP-EP	Yes
	289 MAPBGA	Yes

1. HSE: After start-up, the HSE core is in WFI.
2. eFLEXPWM channels assumed evenly split between 2 instances
3. eMIOS0: 6 channels in PWM mode @ 20 KHz.
4. SAR and SD-ADC represents number of active instances.

6.7 Cyclic wake-up current

The cyclic wake-up current is the calculated average current consumption during the periodic switching between RUN mode and STANDBY mode. This average current can be calculated with the following formula:

ICYCL = RUN Current According to Ratio + STANDBY Current According to Ratio

Where the Current According to Ratio value is calculated as follows:

Current According to Ratio = Supply Current × Ratio of Duration

As an example, the following data represents a case where the code is running a code in RUN mode and spending rest of the time in STANDBY mode. The numbers in table below are representative only, and the Standby IDD numbers must be matched from the IDD tables.

Chip	Device Operating Mode	Supply Current[1] [µA]	Duration [2] [ms]	Ratio of Duration [3]	Current According to Ratio [4] [µA]	ICYCL - Average current [5] [µA]
S32K396	RUN	20000	0.2	0.005	100	159.7
	STANDBY	60	39.8	0.995	59.7	

1. The supply current is obtained through the measurements of the current during the corresponding operating mode.
2. The duration is defined by the application (how much time will the device spend in the according operating mode).
3. The ratio of duration is obtained by dividing the duration of the corresponding operating mode by the total duration of the application.
4. The current according to ratio is obtained by multiplying the supply current and the ratio of duration related to the proper operating mode.
5. The average current is calculated by the addition of each device operating mode's current according to ratio.

7 I/O parameters

7.1 GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)

The leakage current on the GPIO pins is specified as a function of the pad type (Standard, Standard Plus, Medium, Fast, or GPI) and the number of Analog functions (CMP and ADC channels) multiplexed per pin.

The "Analog Function Count" is defined from the number of CMP and ADC channels multiplexed to a given pin. This information can be obtained from the "Direct Signals" column in the IOMUX files attached to the Reference Manual. The "Analog Function Count" is shown in the Condition column of the following table.

Table 17. GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high level DC voltage threshold	0.70 x VDD_HV_A/B	—	VDD_HV_A/B + 0.3	V	VDD_HV_A/B = 3.3V	—
VIL	Input low level DC voltage threshold	VSS - 0.3	—	0.30 x VDD_HV_A/B	V	VDD_HV_A/B = 3.3V	—
WFRST	RESET Input Filtered pulse width [1]	—	—	33	ns	—	—
WNFRST	RESET Input not filtered pulse width [2]	100	—	—	ns	—	—
ILKG_33_S0	3.3V input leakage current for Standard GPIO [3]	-181	—	600	nA	Pins with Analog Function Count = 0	—
ILKG_33_S1	3.3V input leakage current for Standard GPIO [3]	-1020	—	870	nA	Pins with Analog Function Count = 1	—
ILKG_33_S2	3.3V input leakage current for Standard GPIO [3]	-1880	—	1140	nA	Pins with Analog Function Count = 2, plus PTA12, PTD1	—
ILKG_33_S3	3.3V input leakage current for Standard GPIO [3]	-2740	—	1410	nA	Pins with Analog Function Count = 3, plus PTD0	—
ILKG_33_SP0	3.3V input leakage current for Standard Plus GPIO and RESET IO [3]	-537	—	1270	nA	Pins with Analog Function Count = 0	—
ILKG_33_SP1	3.3V input leakage current for Standard Plus GPIO and RESET IO [3]	-1270	—	1530	nA	Pins with Analog Function Count = 1	—
ILKG_33_SP2	3.3V input leakage current for Standard Plus GPIO and RESET IO [3]	-2130	—	1800	nA	Pins with Analog Function Count = 2	—
ILKG_33_M0	3.3V GPIO input leakage current for Medium GPIO [3]	-1300	—	1630	nA	Pins with Analog Function Count = 0	—
ILKG_33_M1	3.3V GPIO input leakage current for Medium GPIO [3]	-1560	—	1900	nA	Pins with Analog Function Count = 1, plus PTC16, PTD5	—

Table continues on the next page...

Table 17. GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ILKG_33_M2	3.3V GPIO input leakage current for Medium GPIO [3]	-2410	—	2170	nA	Pins PTD6 and PTE8	—
ILKG_33_F0	3.3V GPIO input leakage current for Fast GPIO [3]	-1860	—	2720	nA	Pins with Analog Function Count = 0	—
ILKG_33_F1	3.3V GPIO input leakage current for Fast GPIO [3]	-2200	—	2990	nA	Pins with Analog Function Count = 1	—
ILKG_33_ TWINANAMUX	3.3V input leakage current for TWINANAMUX	-0.98	—	0.7	µA	—	—
VHYS_33	Input hysteresis voltage [4]	0.06 x VDD_HV_A/B	—	—	mV	Always Enabled	—
CIN	GPIO Input capacitance	2	4	6	pF	add 2pF for package/ parasitic	—
IPU_33	3.3V GPIO pull up/ down resistance	20	—	60	kΩ	pull up @ 0.3 x VDD_ HV_A/B, pull down @ 0.7 x VDD_HV_A/B	—
IOH_33_S	3.3V output high current for Standard GPIO [5,6]	1.0	—	—	mA	VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_SP	3.3V output high current for Standard Plus GPIO and RESET IO [5,6]	1.5	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_M	3.3V output high current for Medium GPIO [5,6]	3	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_F	3.3V output high current for Fast GPIO [5,6]	4.5	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_SP	3.3V output high current for Standard Plus GPIO and RESET IO [5,6]	3	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_M	3.3V output high current for Medium GPIO [5,6]	6	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—

Table continues on the next page...

Table 17. GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IOH_33_F	3.3V output high current for Fast GPIO [5,6]	9	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOL_33_S	3.3V output low current for Standard GPIO [5,6]	1.0	—	—	mA	VOL <= 0.7V	—
IOL_33_SP	3.3V output low current for Standard Plus GPIO and RESET IO [5,6]	1.5	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_33_M	3.3V output low current for Medium GPIO [5,6]	3.0	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_33_F	3.3V output low current for Fast GPIO [5,6]	4.5	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_33_SP	3.3V output low current for Standard Plus GPIO and RESET IO [5,6]	3	—	—	mA	DSE =1, VOL <= 0.7V	—
IOL_33_M	3.3V output low current for Medium GPIO [5,6]	6	—	—	mA	DSE =1, VOL <= 0.7V	—
IOL_33_F	3.3V output low current for Fast GPIO [5,6]	9	—	—	mA	DSE =1, VOL <= 0.7V	—
FMAX_33_S	3.3V maximum frequency for Standard GPIO [5,7]	—	—	10	MHz	2.9V - 3.6V CL(max) = 25pF	—
FMAX_33_SP	3.3V maximum frequency for Standard Plus GPIO [5,7]	—	—	25	MHz	2.9V - 3.6V CL (max) = 25pF	—
FMAX_33_M	3.3V maximum frequency for Medium GPIO [5,7]	—	—	50	MHz	2.9V - 3.6V CL (max) = 25pF	—
FMAX_33_F	3.3V maximum frequency for Fast GPIO [5,7]	—	—	120	MHz	2.9V - 3.6V CL (max) = 25pF	—
IOHT	Output high current total for all ports [8]	—	—	100	mA	—	—

1. Maximum length of RESET pulse will be filtered by an internal filter on this pin.
2. Minimum length of RESET pulse, guaranteed not to be filtered by the internal filter.

3. A positive value is leakage flowing into pin with pin at VDD_HV_A/B (the GPIO supply level); a negative value is leakage flowing out the pin with the pin at ground.
4. Hysteresis spec does not apply to fast pad
5. GPIO output transition time information can be obtained from the device IBIS model. IBIS models are recommended for system level simulations, as discrete values for I/O transition times are not representative of the I/O pad behavior when connected to an actual transmission line load.
6. I/O output current specifications are valid for the given reference load figure, and the constraints given in the Operating Conditions of this document.
7. I/O timing specifications are valid for the un-terminated 50ohm transmission line reference load given in the figure below. A lumped 8pF load is assumed in addition to a 5 inch microstrip trace on standard FR4 with approximately 3.3pF/inch. For signals with frequency greater than 63MHz, a maximum 2 inch PCB trace is assumed. For best signal integrity, the series resistance in the transmission line should be matched closely to the selected output resistance (ROUT_*) of the I/O pad.
8. To determine total switching current on any I/O supply, current values per output pin should not be incrementally summed. I/O interfaces on the device are asynchronous to each other, so not all switching occurs at the same instant. Actual use case must be considered.

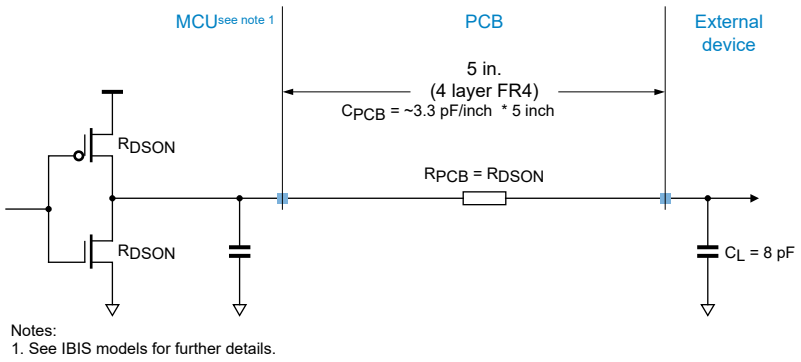

Figure 8. Reference Load Diagram

7.2 GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)

The leakage current on the GPIO pins is specified as a function of the pad type (Standard, Standard Plus, Medium, Fast, or GPI) and the number of Analog functions (CMP and ADC channels) multiplexed per pin.

The "Analog Function Count" is defined from the number of CMP and ADC channels multiplexed to a given pin. This information can be obtained from the "Direct Signals" column in the IOMUX files attached to the Reference Manual. The "Analog Function Count" is shown in the Condition column of the following table.

Table 18. GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high level DC voltage threshold	0.65 x VDD_HV_A/B	—	VDD_HV_A/B + 0.3	V	VDD_HV_A/B = 5.0V	—
VIL	Input low level DC voltage threshold	VSS - 0.3	—	0.35 x VDD_HV_A/B	V	VDD_HV_A/B = 5.0V	—
WFRST	RESET Input filtered pulse width [1]	—	—	33	ns	—	—
WNFRST	RESET Input not filtered pulse width [2]	100	—	—	ns	—	—

Table continues on the next page...

Table 18. GPIO DC electrical specifications, 5.0V (4.5V - 5.5V) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ILKG_50_S0	5.0V input leakage current for Standard GPIO [3]	-250	—	800	nA	Pins with Analog Function Count = 0	—
ILKG_50_S1	5.0V input leakage current for Standard GPIO [3]	-1300	—	1100	nA	Pins with Analog Function Count = 1	—
ILKG_50_S2	5.0V input leakage current for Standard GPIO [3]	-2300	—	1450	nA	Pins with Analog Function Count = 2, plus PTA12, PTD1	—
ILKG_50_S3	5.0V input leakage current for Standard GPIO [3]	-3300	—	1750	nA	Pins with Analog Function Count = 3, plus PTD0	—
ILKG_50_SP0	5.0V input leakage current for Standard Plus GPIO and RESET IO [3]	-660	—	1760	nA	Pins with Analog Function Count = 0	—
ILKG_50_SP1	5.0V input leakage current for Standard Plus GPIO and RESET IO [3]	-1510	—	2030	nA	Pins with Analog Function Count = 1	—
ILKG_50_SP2	5.0V input leakage current for Standard Plus GPIO and RESET IO [3]	-2450	—	2290	nA	Pins with Analog Function Count = 2	—
ILKG_50_M0	5.0V input leakage current for Medium GPIO [3]	-1615	—	2270	nA	Pins with Analog Function Count = 0	—
ILKG_50_M1	5.0V input leakage current for Medium GPIO [3]	-1970	—	2540	nA	Pins with Analog Function Count = 1, plus PTC16,PTD5	—
ILKG_50_M2	5.0V input leakage current for Medium GPIO [3]	-2830	—	2810	nA	Pins PTD6 and PTE8	—
ILKG_50_F0	5.0V input leakage current for Fast GPIO [3]	-2120	—	3790	nA	Pins with Analog Function Count = 0	—
ILKG_50_F1	5.0V input leakage current for Fast GPIO [3]	-2980	—	4060	nA	Pins with Analog Function Count = 1	—
ILKG_50_ TWINANAMUX	5.0V input leakage current for TWINANAMUX	-1.1	—	1.1	µA	—	—

Table continues on the next page...

Table 18. GPIO DC electrical specifications, 5.0V (4.5V - 5.5V) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VHYS_50	input hysteresis voltage [4]	0.06 x VDD_HV_A/B	—	—	mV	Always enabled	—
CIN	GPIO Input capacitance	2	4	6	pF	add 2pF for package/ parasitic	—
IPU_50	5.0V GPIO pull up/ down resistance	20	—	55	kΩ	pull up @ 0.3 * VDD_HV_*, pull down @ 0.7 * VDD_HV_*	—
IOH_50_S	5.0V output high current Standard GPIO [5,6]	1.6	—	—	mA	VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_SP	5.0V output high current Standard Plus GPIO and RESET IO [5,6]	2.5	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_M	5.0V output high current for Medium GPIO [5,6]	4.0	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_F	5.0V output high current for Fast GPIO [5,6]	6.0	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_SP	5.0V output high current for Standard Plus GPIO and RESET IO [5,6]	5.0	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_M	5.0V output high current for Medium GPIO [5,6]	8.0	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_F	5.0V GPIO output high current for Fast GPIO [5,6]	12.0	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOL_50_S	5.0V output low current for Standard GPIO [5,6]	1.6	—	—	mA	VOL <= 0.7V	—
IOL_50_SP	5.0V output low current for Standard Plus GPIO and RESET IO [5,6]	2.5	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_50_M	5.0V output low current for Medium GPIO [5,6]	4.0	—	—	mA	DSE =0, VOL <= 0.7V	—

Table continues on the next page...

Table 18. GPIO DC electrical specifications, 5.0V (4.5V - 5.5V) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IOL_50_F	5.0V output low current for Fast GPIO [5,6]	6.0	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_50_SP	5.0V output low current for Standard Plus GPIO and RESET IO [5,6]	5.0	—	—	mA	DSE =1, VOL <= 0.7V	—
IOL_50_M	5.0V output low current for medium GPIO [5,6]	8.0	—	—	mA	DSE =1, VOL <= 0.7V	—
IOL_50_F	5.0V output low current for Fast GPIO [5,6]	12.0	—	—	mA	DSE =1, VOL <= 0.7V	—
FMAX_50_S	5.0V maximum frequency for Standard GPIO [5,7]	—	—	10	MHz	3.6V - 5.5V CL (max) = 25pF	—
FMAX_50_SP	5.0V maximum frequency for Standard Plus GPIO [5,7]	—	—	25	MHz	3.6V - 5.5V CL (max) = 25pF	—
FMAX_50_M	5.0V maximum frequency for Medium GPIO [5,7]	—	—	25	MHz	3.6V - 5.5V CL (max) = 25pF	—
FMAX_50_F	5.0V maximum frequency for Fast GPIO [5,7]	—	—	25	MHz	3.6V - 5.5V CL (max) = 25pF	—
IOHT	Output high current total for all ports [8]	—	—	100	mA	—	—

1. Maximum length of RESET pulse will be filtered by an internal filter on this pin.
2. Minimum length of RESET pulse, guaranteed not to be filtered by the internal filter.
3. A positive value is leakage flowing into pin with pin at VDD_HV_A/B (the GPIO supply level); a negative value is leakage flowing out the pin with the pin at ground.
4. Hysteresis spec does not apply to fast pad
5. GPIO output transition time information can be obtained from the device IBIS model. IBIS models are recommended for system level simulations, as discrete values for I/O transition times are not representative of the I/O pad behavior when connected to an actual transmission line load.
6. I/O output current specifications are valid for the given reference load figure, and the constraints given in the Operating Conditions of this document.
7. I/O timing specifications are valid for the un-terminated 50ohm transmission line reference load given in the figure below. A lumped 8pF load is assumed in addition to a 5 inch microstrip trace on standard FR4 with approximately 3.3pF/inch.. For best signal integrity, the series resistance in the transmission line should be matched closely to the selected output resistance (ROUT_*) of the I/O pad.
8. To determine total switching current on any I/O supply, current values per output pin should not be incrementally summed. I/O interfaces on the device are asynchronous to each other, so not all switching occurs at the same instant. Actual use case must be considered.

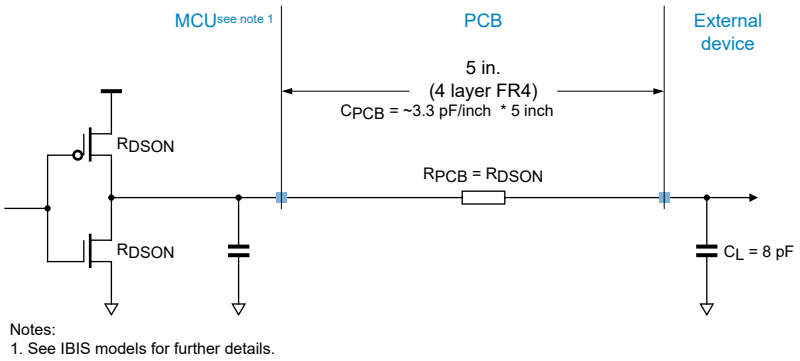

Figure 9. Reference Load Diagram

7.3 3.3V (2.97V - 3.63V) GPIO Output AC Specification

Table 19. 3.3V (2.97V - 3.63V) GPIO Output AC Specification

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TR_TF_33_S	3.3V Standard GPIO rise/fall time [1,2,3]	5	—	28	ns	CL (max) = 25pF	—
TR_TF_33_S	3.3V Standard GPIO rise/fall time [1,2,3]	9.5	—	43	ns	CL (max) = 50pF	—
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time [1,2,3]	4	—	17.5	ns	DSE=0 CL (max) = 25pF	—
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time [1,2,3]	1.9	—	10	ns	DSE=1 CL (max) = 25pF	—
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time [1,2,3,4]	7.5	—	27	ns	DSE=0 CL (max) = 50pF	—
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time [1,2,3,4]	3.5	—	15	ns	DSE=1 CL (max) = 50pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time [1,2,3]	2.2	—	12.3	ns	DSE=0, SRE=0 CL (max) = 25pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time [1,2,3]	3.0	—	14	ns	DSE=0, SRE=1 CL (max) = 25pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time [1,2,3]	0.8	—	6.6	ns	DSE=1, SRE=0 CL (max) = 25pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time [1,2,3]	2.4	—	10.5	ns	DSE=1, SRE=1 CL (max) = 25pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time [1,2,3,4]	4.5	—	17.3	ns	DSE=0, SRE=0 CL (max) = 50pF	—

Table continues on the next page...

Table 19. 3.3V (2.97V - 3.63V) GPIO Output AC Specification (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TR_TF_33_M	3.3V Medium GPIO rise/fall time [1,2,3,4]	5	—	19.8	ns	DSE=0, SRE=1 CL (max) = 50pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time [1,2,3,4]	2.2	—	10	ns	DSE=1, SRE=0 CL (max) = 50pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time [1,2,3,4]	3.6	—	13.9	ns	DSE=1, SRE=1 CL (max) = 50pF	—
TR_TF_33_F	3.3V Fast GPIO rise/fall time [1,2,3]	0.5	—	4.9	ns	DSE=0, SRE=0 CL (max) = 25pF	—
TR_TF_33_F	3.3V Fast GPIO rise/fall time [1,2,3]	2.1	—	10	ns	DSE=0, SRE=1 CL (max) = 25pF	—
TR_TF_33_F	3.3V Fast GPIO rise/fall time [1,2,3]	0.4	—	2.2	ns	DSE=1, SRE=0 CL (max) = 25pF	—
TR_TF_33_F	3.3V Fast GPIO rise/fall time [1,2,3]	1.2	—	7.1	ns	DSE=1, SRE=1 CL (max) = 25pF	—
TR_TF_33_F	3.3V Fast GPIO rise/fall time [1,2,3,4]	1.1	—	8	ns	DSE=0, SRE=0 CL (max) = 50pF	—
TR_TF_33_F	3.3V Fast GPIO rise/fall time [1,2,3,4]	2.6	—	12.1	ns	DSE=0, SRE=1 CL (max) = 50pF	—
TR_TF_33_F	3.3V Fast GPIO rise/fall time [1,2,3,4]	0.8	—	4.2	ns	DSE=1, SRE=0 CL (max) = 50pF	—
TR_TF_33_F	3.3V Fast GPIO rise/fall time [1,2,3,4]	1.5	—	8.6	ns	DSE=1, SRE=1 CL (max) = 50pF	—

1. I/O timing specifications are valid for the un-terminated 50ohm transmission line reference load given in the figure below. A lumped 8pF load (typical) is assumed at the end of a 5 inch microstrip trace on standard FR4 with approximately 3.3pF/inch. For signals with frequency greater than 63MHz, a maximum 2 inch PCB trace is assumed. For best signal integrity, the series resistance in the transmission line should be matched closely to the selected output resistance (ROUT_*) of the I/O pad.
2. GPIO rise/fall time specifications are derived from simulation model for the defined operating points (between 20% and 80% of VDD_HV_A/B level). Actual application rise/fall time should be extracted from IBIS model simulations with the microcontroller models and application PCB.
3. GPIO output transistion time information can be obtained from the device IBIS model. IBIS models are recommended for system level simulations, as discrete values for I/O transition times are not representative of the I/O pad behavior when connected to an actual transmission line load.
4. Output timing valid for maximum external load C L = 50pF (includes PCB trace, package trace, and external device input load).

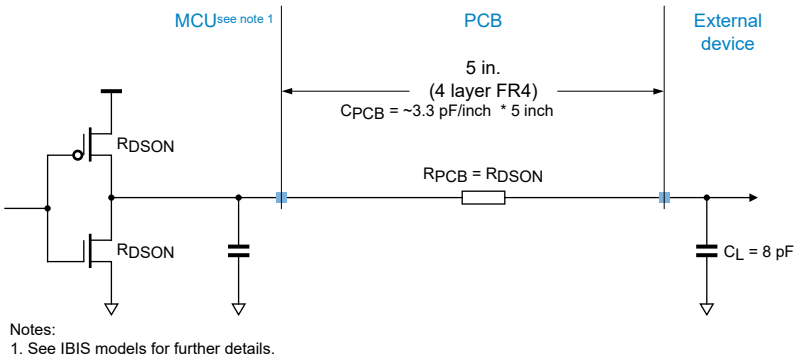

Figure 10. Reference Load Diagram

7.4 5.0V (4.5V - 5.5V) GPIO Output AC Specification

Table 20. 5.0V (4.5V - 5.5V) GPIO Output AC Specification

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TR_TF_50_S	5.0V Standard GPIO rise/fall time [1,2,3]	5	—	21	ns	CL (max) = 25pF	—
TR_TF_50_S	5.0V Standard GPIO rise/fall time [1,2,3,4]	8.5	—	31	ns	CL (max) = 50pF	—
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time [1,2,3]	3	—	13.2	ns	DSE=0 CL (max) = 25pF	—
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time [1,2,3]	1	—	7.1	ns	DSE=1 CL (max) = 25pF	—
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time [1,2,3,4]	6.4	—	18.8	ns	DSE=0 CL (max) = 50pF	—
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time [1,2,3,4]	3.4	—	11	ns	DSE=1 CL (max) =50pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time [1,2,3]	1.8	—	8.2	ns	DSE=0, SRE=0 CL (max) = 25pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time [1,2,3]	2.5	—	9.8	ns	DSE=0, SRE=1 CL (max) = 25pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time [1,2,3]	0.7	—	4.5	ns	DSE=1, SRE=0 CL (max) = 25pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time [1,2,3]	1.8	—	7.2	ns	DSE=1, SRE=1 CL (max) = 25pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time [1,2,3,4]	3.95	—	13.2	ns	DSE=0, SRE=0 CL (max) = 50pF	—

Table continues on the next page...

Table 20. 5.0V (4.5V - 5.5V) GPIO Output AC Specification (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TR_TF_50_M	5.0V Medium GPIO rise/fall time [1,2,3,4]	4.3	—	13.8	ns	DSE=0, SRE=1 CL (max) = 50pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time [1,2,3,4]	1.6	—	7.1	ns	DSE=1, SRE=0 CL (max) = 50pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time [1,2,3,4]	2.7	—	9.6	ns	DSE=1, SRE=1 CL (max) = 50pF	—
TR_TF_50_F	5.0V Fast GPIO rise/fall time [1,2,3]	0.4	—	3.15	ns	DSE=0, SRE=0 CL (max) = 25pF	—
TR_TF_50_F	5.0V Fast GPIO rise/fall time [1,2,3]	1.5	—	6.7	ns	DSE=0, SRE=1 CL (max) = 25pF	—
TR_TF_50_F	5.0V Fast GPIO rise/fall time [1,2,3]	0.3	—	2.02	ns	DSE=1, SRE=0 CL (max) = 25pF	—
TR_TF_50_F	5.0V Fast GPIO rise/fall time [1,2,3]	0.9	—	4.85	ns	DSE=1, SRE=1 CL (max) = 25pF	—
TR_TF_50_F	5.0V Fast GPIO rise/fall time [1,2,3,4]	1.0	—	5.8	ns	DSE=0, SRE=0 CL (max) = 50pF	—
TR_TF_50_F	5.0V Fast GPIO rise/fall time [1,2,3,4]	1.9	—	8.5	ns	DSE=0, SRE=1 CL (max) = 50pF	—
TR_TF_50_F	5.0V Fast GPIO rise/fall time [1,2,3,4]	0.9	—	3.0	ns	DSE=1, SRE=0 CL (max) = 50pF	—
TR_TF_50_F	5.0V Fast GPIO rise/fall time [1,2,3,4]	1.3	—	6.1	ns	DSE=1, SRE=1 CL (max) = 50pF	—

1. I/O timing specifications are valid for the un-terminated 50ohm transmission line reference load given in the figure below. A lumped 8pF load (typical) is assumed at the end of a 5 inch microstrip trace on standard FR4 with approximately 3.3pF/inch. For best signal integrity, the series resistance in the transmission line should be matched closely to the selected output resistance (ROUT_*) of the I/O pad.
2. GPIO output transistion time information can be obtained from the device IBIS model. IBIS models are recommended for system level simulations, as discrete values for I/O transition times are not representative of the I/O pad behavior when connected to an actual transmission line load.
3. GPIO rise/fall time specifications are derived from simulation model for the defined operating points (between 20% and 80% of VDD_HV_A/B level). Actual application rise/fall time should be extracted from IBIS model simulations with the microcontroller models and application PCB.
4. Output timing valid for maximum external load C L = 50pF (includes PCB trace, package trace, and external device input load).

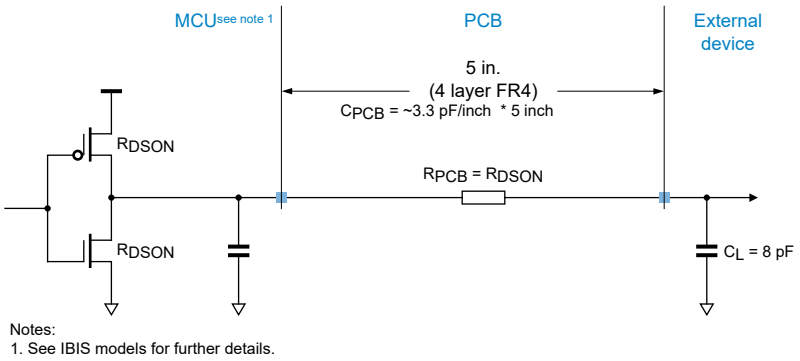

Figure 11. Reference Load Diagram

8 Real-time control

8.1 eTPU timing

Table 21. eTPU timing

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tICPW	eTPU input channel pulse width [1,2]	4	—	—	tPER_CLK	—	—
tOCPW	eTPU output channel pulse width [1,2]	1	—	—	tPER_CLK	—	—

1. tPER_CLK is the period of the peripheral clock (PER_CLK) on the device.
2. Value in the table represent the minimum pulse which is the module capable to process. When the input signal is going from the pins there can be limitation done by the pin parameters and its external circuity

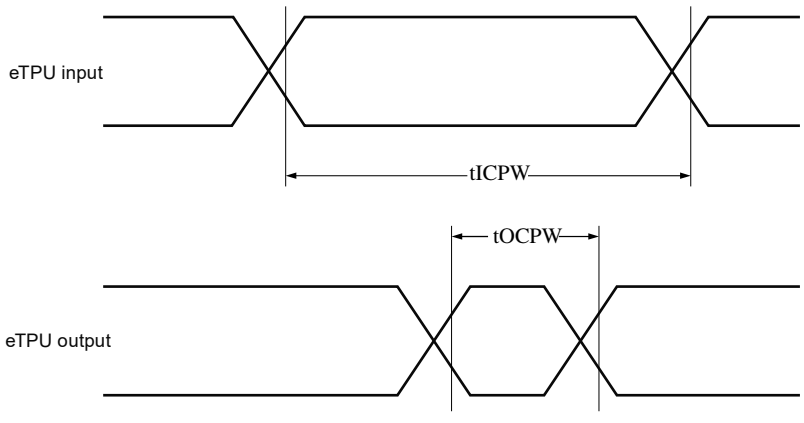

Figure 12. eTPU timing

8.2 eTPU skew characteristics

Table 22. eTPU skew characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSCP	Skew in Complementary Pair [1]	—	—	3	ns	—	—
tTS	Total Skew [2]	—	—	13	ns	—	—

1. etpu_A channels only PTC8/PTC29 , PTA7/PTC30 , PTA6/PTC31 , PTD20/PTB16, PTB15/PTB14 , PTD21/PTB13 , PTD3/PTD2 , PTD23/PTA3 , PTA2/PTD24
2. etpu_A channels only Group1 (PTC8/PTC29, PTA7/PTC30, PTA6/PTC31), Group2(PTD20/PTB16, PTB15/PTB14, PTD21/PTB13) and Group3 (PTD3/PTD2, PTD23/PTA3, PTA2/PTD24)

8.3 eMIOS

Table 23. eMIOS

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tMIPW	eMIOS input pulse width [1,2]	4	—	—	tPER_CLK	—	—
tMOPW	eMIOS output pulse width [1,2,3]	1	—	—	tPER_CLK	—	—

1. tPER_CLK is the period of the peripheral clock (PER_CLK) on the device.
2. Value in the table represent the minimum pulse which is the module capable to process. When the input signal is going from the pins there can be limitation done by the pin parameters and its external circuity
3. Actual output pulse may be larger when considering a slow transitioning output.

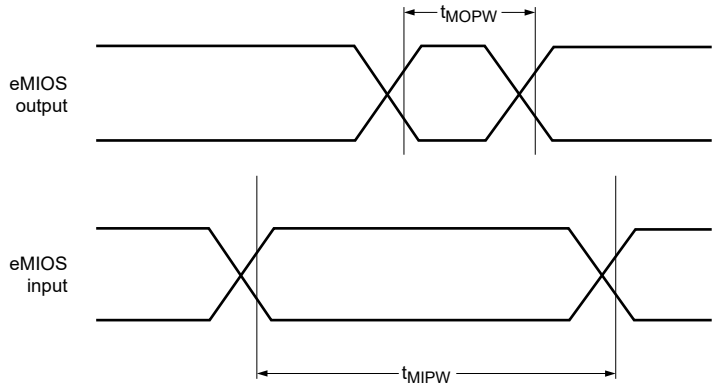

Figure 13. EMIOS Timing

8.4 LCU

Table 24. LCU

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tMIPW	LCU input pulse width [1,2]	4	—	—	tPER_CLK	—	—
tMOPW	LCU output pulse width [1,2,3]	1	—	—	tPER_CLK	—	—

1. tPER_CLK is the period of the peripheral clock (PER_CLK) on the device.
2. Value in the table represent the minimum pulse which is the module capable to process. When the input signal is going from the pins there can be limitation done by the pin parameters and its external circuity
3. Actual output pulse may be larger when considering a slow transitioning output.

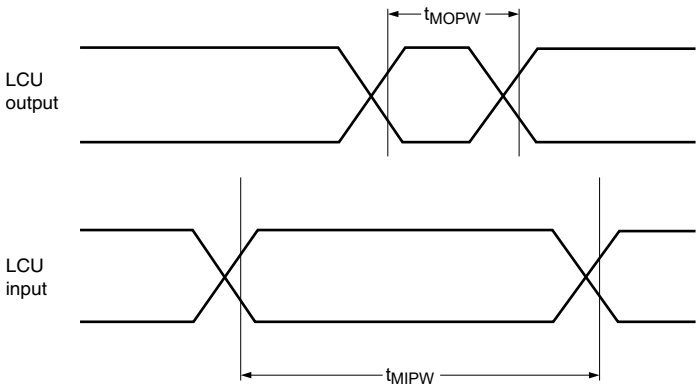

Figure 14. LCU timing

8.5 LCU skew characteristics

Table 25. LCU skew characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSCP	Skew in Complementary Pair [1]	—	—	3	ns	—	—
tTS	Total Skew [2]	—	—	13	ns	—	—

1. Pairs (For LCU_0 (PTD20/PTB16, PTB15/PTB14, PTD21/PTB13)), For LCU_1 (PTC28/PTC9 , PTC8 /PTC29, PTA7/ PTC30, PTA6/PTC31))
2. LCU_0 group:(PTD20/PTB16, PTB15/PTB14, PTD21/PTB13), LCU_1 group: (PTC28 /PTC9 , PTC8/ PTC29, PTA7/ PTC30, PTA6/PTC31)

9 Glitch Filter

Table 26. Glitch Filter

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TFILT	Glitch filter max filtered pulse width [1,2,3]	—	—	20	ns	—	—
TUNFILT	Glitch filter min unfiltered pulse width [2,3,4]	400	—	—	ns	—	—

1. Pulses shorter than defined by the maximum value are guaranteed to be filtered (not passed).
2. An input signal pulse is defined by the duration between the input signal's crossing of a Vil/Vih threshold voltage level, and the next crossing of the opposite level.
3. Pulses in between the max filtered and min unfiltered may or may not be passed through.
4. Pulses larger than defined by the minimum value are guaranteed to not be filtered (passed).

10 LVDS specifications

10.1 LVDS 3.3V Receiver Electrical Specifications

These specifications are related to LVDS pads dedicated to Zipwire.

Table 27. LVDS 3.3V Receiver Electrical Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Dmax	Maximum Data Rate	—	—	480	Mbps	—	—
VID	Input differential signal swing	100	—	400	mV	—	—
VICM	Input signal common mode	0.2	—	1.8	V	—	—
Duty Cycle	Duty Cycle on Core side port for a 50% duty cycle input differential	40	—	60	%	—	—
Rterm	On die termination resistance	80	100	135	Ohm	—	—
Tstart	Startup Time	—	—	1	us	—	—
Vfault_fall	pad_p,pad_n voltage threshold below which open driver detection asserts the fault indicator	50	—	200m	mV	—	—
Vfault_rise	pad_p,pad_n voltage threshold above which open driver	50	—	200m	mV	—	—

Table continues on the next page...

Table 27. LVDS 3.3V Receiver Electrical Specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	detection de-asserts the fault indicator						
Ipin_leakage_ disabled	Pin Leakage with Receiver disabled	-5	—	5	uA	—	—
Ipin_leakge_ enabled	Pin Leakage with Receiver enabled	-5	—	100	uA	—	—
IDD_VDD33_RUN	VDD33 current consumption when enabled	—	—	3	mA	—	—

10.2 LVDS 3.3V Transmitter Electrical Specifications

These specifications are related to LVDS pads dedicated to Zipwire.

Table 28. LVDS 3.3V Transmitter Electrical Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Dmax	Maximum Data Rate	—	—	480	Mbps	—	—
VOD	Output differential swing	200	300	450	mV	—	—
VCM	Output Common Mode	1.1	1.2	1.3	V	—	—
VOH	Output High Indicator	VCM+100m	—	—	V	—	—
VOL	Output Low indicator	—	—	VCM-100m	V	—	—
Dj	Deterministic Jitter through the LVDS Tx I/O	—	—	100	ps	—	—
Ipin_leakage	Pin Leakage(disabled condition)	-5	—	5	uA	—	—
IDD_VDD33_RUN	VDD33 current consumption when enabled	—	—	7	mA	—	—
—	Startup Time	—	—	1	us	—	—
Cload	Max load specification	—	—	10	pF	—	—
Ztline	pad_p , pad_n board Tline impedance	47.5	50	52.5	Ohm	—	—

10.3 LVDS 5V Transmitter Electrical Specifications

These specifications are related to LVDS pads dedicated to MSC.

Table 29. LVDS 5V Transmitter Electrical Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Dmax	Maximum Data Rate	—	—	80	Mbps	—	—
VOD	Output differential swing	200	300	400	mV	—	—
VCM	Output Common Mode	1.1	1.2	1.3	V	—	—
VOH	Output High Indicator	VCM+100m	—	—	V	—	—
VOL	Output Low indicator	—	—	VCM-100m	V	—	—
Dj	Determinstic jitter through the LVDS Tx I/O	—	—	250	ps	—	—
Ipin_leakage	Pin Leakage(disabled condition)	-5.6	—	5.6	uA	—	—
IDD_VDDE_RUN	VDDE current consumption when enabled	—	—	7.5	mA	—	—
Cload	Max load specification	—	—	10	pF	—	—
Ztline	pad_p,pad_n board Tline impedance	47.5	50	52.5	Ohm	—	—
ZTLDIFF	Transmission line differential impedance	95	100	105	Ohm	—	—

11 eFlexPWM

Table 30. eFlexPWM

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fref	Input Clock frequency	—	320	—	MHz	—	—
Tdelay	PWM Delay Resolution	—	195	—	ps	—	—
Tlock	DLL Lock Time	—	—	25	us	—	—
IVDD	Current Consumption	—	—	8	mA	only for single instance of PWM	—

11.1 eFlexPWM skew characteristics

Table 31. eFlexPWM skew characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSCP	Skew in Complementary Pair [1]	—	—	3	ns	—	—
tTS	Total Skew [2]	—	—	13	ns	—	—

1. Pairs(For PWM_0:(PTD4/PTD22, PTD2/PTD3 , PTA3/PTD23, PTD24/PTA2), For PWM_1:(PTC9/PTC28, PTC29/PTC8, PTC30/PTA7, PTC31/PTA6))
2. PWM_0 group:(PTD4/PTD22, PTD2/PTD3 , PTA3/PTD23, PTD24/PTA2), For PWM_1 group: (PTC9/PTC28, PTC29/PTC8, PTC30/PTA7, PTC31/PTA6)

12 Flash memory specification

12.1 Flash memory program and erase specifications

Table 32. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3,4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 100,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	102	122	129	111	150		µs
t_{ppgm}	Page (256 bits) program time	142	171	180	157	200		µs
t_{qppgm}	Quad-page (1024 bits) program time	314	377	396	341	450		µs
t_{8kpgm}	8 KB Sector program time	20	24	26	22	30		ms
t_{8kers}	8 KB Sector erase time	4.8	8.5	10.6	6.5	30		ms
$t_{256kbers}$	256KB Block erase time	22.8	27.4	28.8	24.4	40	—	ms
$t_{512kbers}$	512KB Block erase time	25.4	30.5	32.1	27.9	45	—	ms
t_{1mbers}	1MB Block erase time	30.6	36.8	38.7	33.6	50	—	ms
t_{2mbers}	2MB Block erase time	41.1	49.3	51.8	45.2	60	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Sector program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 25 cycles, nominal voltage.

4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤T_J ≤150°C, full spec voltage.

12.2 Flash memory Array Integrity and Margin Read specifications

Table 33. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1] [2]	Units[3]
$t_{ai256kseq}$	Array Integrity time and Margin Read time for sequential sequence on 256KB block.	—	—	8192 x Tperiod x Nread (plus 40uS adder required if User Margin Read)	—
$t_{ai512kseq}$	Array Integrity time and Margin Read time for sequential sequence on 512KB block.	—	—	16384 x Tperiod x Nread (plus 40uS adder required if User Margin Read)	—
$t_{ai1mseq}$	Array Integrity time and Margin Read time for sequential sequence on 1MB block.	—	—	32768 x Tperiod x Nread (plus 40uS adder required if User Margin Read)	—
$t_{ai2mseq}$	Array Integrity time and Margin Read time for sequential sequence on 2MB block.	—	—	65536 x Tperiod x Nread (plus 40uS adder required if User Margin Read)	—
$t_{ai256kprop}$	Array Integrity time for proprietary sequence on 256KB block.	—	—	106496 x Tperiod x Nread	—
$t_{ai512kprop}$	Array Integrity time for proprietary sequence on 512KB block.	—	—	229376 x Tperiod x Nread	—
$t_{ai1mprop}$	Array Integrity time for proprietary sequence on 1MB block.	—	—	491520 x Tperiod x Nread	—
$t_{ai2mprop}$	Array Integrity time for proprietary sequence on 2MB block.	—	—	1048576 x Tperiod x Nread	—

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including single read, dual read, quad read contribution. Thus for a read setup that requires 6 clocks to read Nread would equal 6.
2. Array Integrity times are actual hardware execution times and do not include software overhead or system code execution overhead.
3. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

12.3 Flash memory module life specifications

Table 34. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 256 KB and 512 KB blocks using Sector Erase.	—	100,000	—	P/E cycles
	Number of program/erase cycles per block for 1 MB and 2 MB blocks using Sector Erase.	—	1,000	—	P/E cycles
	Number of program/erase cycles per block using Block Erase[1]	—	25	—	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	20	—	Years
		Blocks with 100,000 P/E cycles.	10	—	Years

1. Program and erase supported for factory conditions. Nominal supply values and operation at 25°C.

12.3.1 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure.

The spec window represents qualified limits.

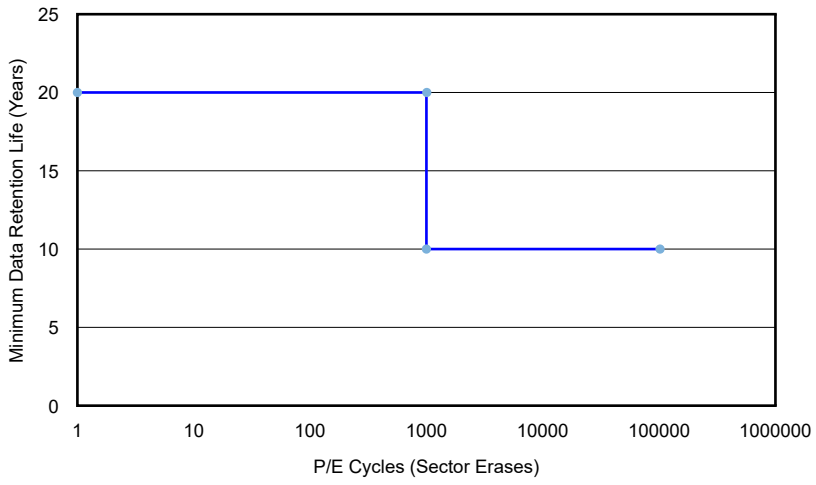

Figure 15. Data retention vs program/erase cycles

12.4 Flash memory AC timing specifications

Table 35. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{done}	Time from 0 to 1 transition on the MCR[EHV] bit initiating a program/erase until the MCR[DONE] bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR[EHV] bit aborting a program/erase until the MCR[DONE] bit is set to a 1.	5 plus four system clock periods	—	22 plus four system clock periods[1]	µs
t_{drcv}	Time to recover once exiting low power mode.	14 plus seven system clock periods[2]	17.5 plus seven system clock periods	21 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0[AIE] initiating a Margin Read or Array Integrity until the UT0[AID] bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing UT0[AISUS] or clearing UT0[NAIBP]	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0[AIE] initiating an Array Integrity abort until the UT0[AID] bit is set. This time also applies to the UT0[AISUS] to UT0[AID] setting in the event of a Array Integrity suspend request.	—	—	50 system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0[AIE] initiating a Margin Read abort until the UT0[AID] bit is set. This time also applies to the UT0[AISUS] to UT0[AID] setting in the event of a Margin Read suspend request.	—	—	26 plus fifteen system clock periods	µs

1. For Block Erase, Tdones times may be 3x max spec.
2. In extreme cases (1 block configurations) Tdrcv min may be faster (12uS plus seven system clocks)

12.5 Flash memory read timing parameters

Table 36. Flash Read Wait State Settings (S32K396, S32K394, S32K376, and S32K374)

Flash Frequency	RWSC setting
250 KHz < Freq ≤ 60 MHz	1
60 MHz < Freq ≤ 90 MHz	2
90 MHz < Freq ≤ 120 MHz	3
120 MHz < Freq ≤ 150 MHz	4
150 MHz < Freq ≤ 180 MHz	5
180 MHz < Freq ≤ 210 MHz	6

Table continues on the next page...

Table 36. Flash Read Wait State Settings (S32K396, S32K394, S32K376, and S32K374) (continued)

Flash Frequency	RWSC setting
210 MHz < Freq ≤ 240 MHz	7
240 MHz < Freq ≤ 250 MHz	8

13 Analog modules

13.1 SAR_ADC

All below specs are applicable only when one ADC instance is in operation and averaging is used or multiple ADC instances are operational at the same time but sampling different channels. Best performance can be achieved if only one ADC is operational at a time sampling one channel

Table 37. SAR_ADC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_HV_A	ADC Supply Voltage [1]	2.97	—	5.5	V	—	—
DVREFL	VSS / VREFL Voltage Difference [2]	-100	—	100	mV	—	—
VAD_INPUT	ADC Input Voltage [3]	VREFL	—	VREFH	V	—	—
fAD_CK	ADC Clock Frequency	10	—	80	MHz	—	—
tSAMPLE	ADC Input Sampling Time	275	—	—	ns	—	—
tCONV	ADC Total Conversion Time	1	—	—	us	12-bit result	—
tCONV	ADC Total Conversion Time	0.9	—	—	us	10-bit result	—
CAD_INPUT	ADC Input Capacitance	—	—	13.8	pF	ADC component plus pad capacitance (~2pF)	—
RAD_INPUT	ADC Input Resistance	—	—	4.6	KΩ	ADC + mux+SOC routing	—
RS	Source Impedance, precision channels	—	20	—	Ω	—	—
RS	Source Impedance, standard channels	—	20	—	Ω	—	—
TUE	ADC Total Unadjusted Error [4,5]	—	+/-4	+/-6	LSB	without adjacent pin current injection	—

Table continues on the next page...

Table 37. SAR_ADC (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TUE	ADC Total Unadjusted Error [5]	—	+/-4	+/-8	LSB	with up to +/-3mA of current injection on adjacent pins	—
IAD_REF	Current Consumption on ADC Reference pin, VREFH.	—	—	200	uA	Per ADC for dedicated or shared reference pins	—
IDDA	Current Consumption on ADC Supply, VDD_HV_A	—	2.1	—	mA	Current consumption per ADC module, ADC enabled and converting	—
CS	Sampling Capacitance	6.4 (gain=0) 9.72 pF(gain=max)	7.36 (gain=0) 11.12 pF(gain=max)	8.32 (gain=0) 12.52 (gain=max)	pF	all channels	—
RAD	Sampling Switch Impedance	80	170	520	Ohm	all channels	—
CP1	Pin capacitance	1.42	—	5.30	pF	all channels	—
CP1	Pin capacitance	1.42	—	4.38	pF	Precision channels	—
CP1	Pin capacitance	1.61	—	5.30	pF	Standard channels	—
CP2	Analog Bus Capacitance	0.32	—	5	pF	all channels	—
CP2	Analog Bus Capacitance	0.32	—	2.2	pF	Precision channels	—
CP2	Analog Bus Capacitance	0.497	—	5	pF	Standard channels	—
RSW1	Channel selection Switch impedance	65.9	—	1410	Ohm	all channels	—
RSW1	Channel selection Switch impedance	65.9	—	712	Ohm	Precision channels	—
RSW1	Channel selection Switch impedance	65.9	—	1410	Ohm	Standard channels	—

1. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC.
2. VSS and VREFL should be shorted on PCB. 100mV difference between VSS and VREFL is for transient only (not for DC).
3. This is ADC Input range for ADC accuracy guaranteed in this input range only. For SoC Pin capability, see Operation Condition Section.
4. Spec valid if potential difference between VDD_HV_A and VREFH should follow VDD_HV_A +0.1V >=VREFH >= VDD_HV_A -1.5V
5. TUE spec for precision and standard channels is based on 12-bit level resolution.

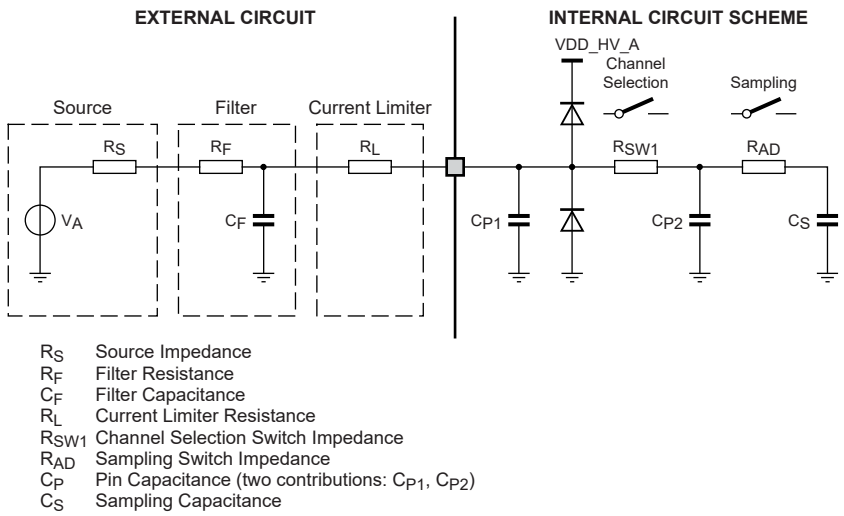

Figure 16. SAR ADC Input Circuit

13.2 Sigma Delta Analog to Digital Converter

Table 38. Sigma Delta Analog to Digital Converter

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VINSE	Peak-to-peak input voltage range, Single-ended	—	VREFP/ GAIN	—	V	Negative input set to 0	—
VINSE	Peak-to-peak input voltage range, Single-ended	—	+/- VREFP/2	—	V	Negative input set to AVDD/2; GAIN=1	—
VINSE	Peak-to-peak input voltage range, Single-ended	—	+/- VREFP/ GAIN	—	V	Negative input set to AVDD/2; GAIN=2, 4, 8, 16	—
VINDIFF	Peak-to-peak input voltage range, differential	—	+/- (VREFP-VREFN)/ GAIN	—	V	—	—
AVDD	Analog power supply	4.5	5.0	5.5	V	—	—
DVDD	Digital power supply	0.99	1.1	1.21	V	—	—
VREFP	External reference positive voltage	AVDD - 0.025	AVDD	AVDD + 0.025	V	—	—
VREFN	External reference negative voltage	—	0	—	V	—	—
CMRR	Common mode rejection ratio	34	—	—	dB	—	—

Table continues on the next page...

Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
R_AAF	Anti aliasing filter - external series resistance	—	5	20	kOhm	—	—
C_AAF	Anti aliasing filter - filter capacitance	180	220	—	pF	—	—
CS	Modulator sampling capacitor	—	—	75 * GAIN	fF	Gain = 1, 2, 4, 8 After input mux switch	—
GAIN	PGA Gain [1]	1	—	16	-	—	—
RES	SDADC resolution	—	16	—	bits	—	—
Fm	Input clock frequency	—	40	44	MHz	—	—
Fs	Modulator sampling frequency [2]	20	40	—	MHz	—	—
Fd	Decimated output conversion frequency	31.25	—	333	kHz	—	—
OSR_EXT	Oversampling ratio for external modulator	—	128	—	-	—	—
OFFSET_ERR	Input referred offset voltage error [3,4]	—	—	10	mV	After calibration	—
GAIN_ERR	Absolute gain error [3,5]	—	—	10	mV	After calibration	—
&RIPPLE	Passband ripple	-1	—	1	%	From 10Hz to 0.33*Fd. Applicable with NXP default FIR filter.	—
SB_ATTEN	Stop band attenuation	40	—	—	dB	From 0.5*Fd to 1.0*Fd. Applicable with NXP default FIR filter.	—
SB_ATTEN	Stop band attenuation	45	—	—	dB	From 1.0*Fd to 1.5*Fd. Applicable with NXP default FIR filter.	—
SB_ATTEN	Stop band attenuation	50	—	—	dB	From 1.5*Fd to 2.0*Fd. Applicable with NXP default FIR filter.	—
SB_ATTEN	Stop band attenuation	55	—	—	dB	From 2.0*Fd to 2.5*Fd. Applicable with NXP default FIR filter.	—

Table continues on the next page...

Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
SB_ATTEN	Stop band attenuation	60	—	—	dB	From 2.5*Fd to Fs / 2. Applicable with NXP default FIR filter.	—
&GROUP	Group delay OSR=120	44.5	—	719.5	1 / Fs	Applicable with NXP default FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	—
&GROUP	Group delay OSR=125	37	—	612	1 / Fs	Applicable with NXP 320ksps special case FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	—
&GROUP	Group delay OSR=140	52	—	839.5	1 / Fs	Applicable with NXP default FIR filter. Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	—
&GROUP	Group delay OSR=160	59.5	—	959.5	1 / Fs	Applicable with NXP default FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	—
&GROUP	Group delay OSR=180	67	—	1079.5	1 / Fs	Applicable with NXP default FIR filter. Min	—

Table continues on the next page...

Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
						= CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	
&GROUP	Group delay OSR=200	74.5	—	1199.5	1 / Fs	Applicable with NXP default FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	—
&GROUP	Group delay OSR=220	82	—	1319.5	1 / Fs	Applicable with NXP default FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	—
&GROUP	Group delay OSR=240	89.5	—	1439.5	1 / Fs	Applicable with NXP default FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	—
&GROUP	Group delay OSR=280	104.5	—	1679.5	1 / Fs	Applicable with NXP default FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes	—

Table continues on the next page...

Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
						DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	
&GROUP	Group delay OSR=320	119.5	—	1919.5	1 / Fs	Applicable with NXP default FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	—
&GROUP	Group delay OSR=360	134.5	—	2159.5	1 / Fs	Applicable with NXP default FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	—
&GROUP	Group delay OSR=400	149.5	—	2399.5	1 / Fs	Applicable with NXP default FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	—
&GROUP	Group delay OSR=440	164.5	—	2639.5	1 / Fs	Applicable with NXP default FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC	—

Table continues on the next page...

Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
						given data transfer to memory delays and CPU processing.	
&GROUP	Group delay OSR=480	179.5	—	2879.5	1 / Fs	Applicable with NXP default FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	—
&GROUP	Group delay OSR=560	209.5	—	3359.5	1 / Fs	Applicable with NXP default FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	—
&GROUP	Group delay OSR=640	239.5	—	3839.5	1 / Fs	Applicable with NXP default FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	—
&GROUP	Group delay OSR=720	269.5	—	4319.5	1 / Fs	Applicable with NXP default FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	—

Table continues on the next page...

Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
&GROUP	Group delay OSR=800	299.5	—	4799.5	1 / Fs	Applicable with NXP default FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	—
&GROUP	Group delay OSR=880	329.5	—	5279.5	1 / Fs	Applicable with NXP default FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	—
&GROUP	Group delay OSR=960	359.5	—	5759.5	1 / Fs	Applicable with NXP default FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	—
&GROUP	Group delay OSR=1120	419.5	—	6719.5	1 / Fs	Applicable with NXP default FIR filter. Min = CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	—
&GROUP	Group delay OSR=1280	479.5	—	7679.5	1 / Fs	Applicable with NXP default FIR filter. Min	—

Table continues on the next page...

Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
						= CIC filter delay only Max = CIC + FIR filter delay Assumes DSP S/W maintains the periodic output rate of the ADC given data transfer to memory delays and CPU processing.	
tLATENCY	Latency between input data and converted output data	—	—	&GROUP	—	Does not apply to mux change.	—
tSETTLING	Output settling time after input mux change	—	—	2 * &GROUP + 2 * (1 / Fd)	—	—	—
tODRECOVERY	Overdrive recovery time	—	—	2 * &GROUP	—	—	—
tSTARTUP	Start up time from power down	—	—	100	us	—	—
IDDA_SDADC	VDDA supply current - ADC	—	0.1	40	uA	per SDADC - powered OFF	—
IDDA_BIAS_GEN	VDDA supply current - Bias Generator	—	0.008	8	uA	BIASGEN- powered OFF	—
IVREF_ADC	VREF current - ADC	-0.85	-0.47	2.85	uA	per SDADC - powered ON with differential input mode	—
IVREF_ADC	VREF current - ADC	-0.7	0.007	0.7	uA	per SDADC - powered OFF	—
IVREF_BIAS	VREF current - Bias Generator	21	21.4	25	uA	BIASGEN- Powered ON	—
IVREF_BIAS	VREF current - Bias Generator	—	0.001	1.1	uA	BIASGEN- Powered OFF	—
IDD_SDADC	VDD supply current - ADC	—	17	38	uA	ADC powered ON	—
IDD_SDADC	VDD supply current - ADC	—	5	28	uA	ADC powered OFF	—
IDD_BIAS_GEN	VDD supply current - Bias Generator	—	4.3	6.1	uA	ADC powered ON	—

Table continues on the next page...

Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IDD_BIAS_GEN	VDD supply current - Bias Generator	—	0.43	6	uA	ADC powered OFF	—
ZDIFF	Differential input impedance, Gain = 1	215	317	380	kOhm	Fs = 40MHz	—
ZDIFF	Differential input impedance, Gain = 2	130	230	276	kOhm	Fs = 40MHz	—
ZDIFF	Differential input impedance, Gain = 4	75	159	191	kOhm	Fs = 40MHz	—
ZDIFF	Differential input impedance, Gain = 8	40	103	124	kOhm	Fs = 40MHz	—
ZDIFF	Differential input impedance, Gain = 16	40	103	124	kOhm	Fs = 40MHz	—
ZDIFF_20M	Differential input impedance GAIN=1 [6]	430	634	760	kOhm	Fs=20 MHz	—
ZDIFF_20M	Differential input impedance GAIN=2 [6]	260	460	552	kOhm	Fs=20 MHz	—
ZDIFF_20M	Differential input impedance GAIN=4 [6]	150	320	382	kOhm	Fs=20 MHz	—
ZDIFF_20M	Differential input impedance GAIN=8 [6]	80	206	248	kOhm	Fs=20 MHz	—
ZDIFF_20M	Differential input impedance GAIN=16 [6]	80	206	248	kOhm	Fs=20 MHz	—
ZCM	Common mode input impedance, Gain = 1	200	244	320	kOhm	Fs = 40MHz	—
ZCM	Common mode input impedance, Gain = 2	120	148	192	kOhm	Fs = 40MHz	—
ZCM	Common mode input impedance, Gain = 4	65	90	106	kOhm	Fs = 40MHz	—
ZCM	Common mode input impedance, Gain = 8	35	48	58	kOhm	Fs = 40MHz	—
ZCM	Common mode input impedance, Gain =16	35	48	58	kOhm	Fs = 40MHz	—

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Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ZCM_20M	Common mode input impedance GAIN=1 [6]	400	488	640	kOhm	Fs=20 MHz	—
ZCM_20M	Common mode input impedance GAIN=2 [6]	240	296	384	kOhm	Fs=20 MHz	—
ZCM_20M	Common mode input impedance GAIN=4 [6]	130	180	212	kOhm	Fs=20 MHz	—
ZCM_20M	Common mode input impedance GAIN=8 [6]	70	96	116	kOhm	Fs=20 MHz	—
ZCM_20M	Common mode input impedance GAIN=16 [6]	70	96	116	kOhm	Fs=20 MHz	—
OSR_INT	Oversampling ratio for internal modulator	120	—	1280	-	Fs=40 MHz	—
OSR_INT_20M	Oversampling ratio for internal modulator [6]	60	—	640	—	Fs=20 MHz	—
SNRDIFF167	Signal to Noise Ratio GAIN=1, Differential [7]	79	—	—	dB	Fs=40 MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter.	—
SNRDIFF167	Signal to Noise Ratio GAIN=2, Differential [7]	77	—	—	dB	Fs=40 MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter.	—
SNRDIFF167	Signal to Noise Ratio GAIN=4, Differential [7]	74	—	—	dB	Fs=40 MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter.	—

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Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
SNRDIFF167	Signal to Noise Ratio GAIN=8, Differential [7]	71	—	—	dB	Fs=40 MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter.	—
SNRDIFF167	Signal to Noise Ratio GAIN=16, Differential [7]	68	—	—	dB	Fs=40 MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter.	—
SNRDIFF167_20M	Signal to Noise Ratio GAIN=1, Differential [6]	76	—	—	dB	Fs=20MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter.	—
SNRDIFF167_20M	Signal to Noise Ratio GAIN=2, Differential [6]	75	—	—	dB	Fs=20MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter.	—
SNRDIFF167_20M	Signal to Noise Ratio GAIN=4, Differential [6]	74	—	—	dB	Fs=20MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter.	—
SNRDIFF167_20M	Signal to Noise Ratio GAIN=8, Differential [6]	71	—	—	dB	Fs=20MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter.	—
SNRDIFF167_20M	Signal to Noise Ratio GAIN=16, Differential [6]	66	—	—	dB	Fs=20MHz, Output rate = 166.7ksps, full-scale 10kHz input,	—

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Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
						integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter.	
SINADDIFF167	Signal to Noise Ratio and Distortion Gain=1, Differential	72	—	—	dB	Fs=40 MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter.	—
SINADDIFF167	Signal to Noise Ratio and Distortion Gain=2, Differential	69	—	—	dB	Fs=40 MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter.	—
SINADDIFF167	Signal to Noise Ratio and Distortion Gain=4, Differential	66	—	—	dB	Fs=40 MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter.	—
SINADDIFF167	Signal to Noise Ratio and Distortion Gain=8, Differential	63	—	—	dB	Fs=40 MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter.	—
SINADDIFF167	Signal to Noise Ratio and Distortion Gain=16, Differential	60	—	—	dB	Fs=40 MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter.	—
SINADDIF167_20M	Signal to Noise Ratio and Distortion Gain=1, Differential [6]	72	—	—	dB	Fs=20MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz.	—

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Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
						Applicable with NXP default FIR filter	
SINADDIF167_20M	Signal to Noise Ratio and Distortion Gain=2, Differential [6]	69	—	—	dB	Fs=20MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter	—
SINADDIF167_20M	Signal to Noise Ratio and Distortion Gain=4, Differential [6]	66	—	—	dB	Fs=20MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter	—
SINADDIF167_20M	Signal to Noise Ratio and Distortion Gain=8, Differential [6]	63	—	—	dB	Fs=20MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter	—
SINADDIF167_20M	Signal to Noise Ratio and Distortion Gain=16, Differential [6]	60	—	—	dB	Fs=20MHz, Output rate = 166.7ksps, full-scale 10kHz input, integration bandwidth up to 55.6kHz. Applicable with NXP default FIR filter	—
SNRSE333	Signal to Noise Ratio GAIN=1, Single-ended [7]	68	—	—	dB	Fs=40 MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SNRSE333	Signal to Noise Ratio GAIN=2, Single-ended [7]	65	—	—	dB	Fs=40 MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—

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Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
SNRSE333	Signal to Noise Ratio GAIN=4, Single-ended [7]	62	—	—	dB	Fs=40 MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SNRSE333	Signal to Noise Ratio GAIN=8, Single-ended [7]	59	—	—	dB	Fs=40 MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SNRSE333	Signal to Noise Ratio GAIN=16, Single-ended [7]	56	—	—	dB	Fs=40 MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SNRSE333_20M	Signal to Noise Ratio GAIN=1, Single-ended [6]	61	—	—	dB	Fs=20MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter	—
SNRSE333_20M	Signal to Noise Ratio GAIN=2, Single-ended [6]	60	—	—	dB	Fs=20MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter	—
SNRSE333_20M	Signal to Noise Ratio GAIN=4, Single-ended [6]	59	—	—	dB	Fs=20MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter	—
SNRSE333_20M	Signal to Noise Ratio GAIN=8, Single-ended [6]	56	—	—	dB	Fs=20MHz, Output rate = 320/333ksps, full-scale 20kHz input,	—

Table continues on the next page...

Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
						integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter	
SNRSE333_20M	Signal to Noise Ratio GAIN=16, Single-ended [6]	50	—	—	dB	Fs=20MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter	—
SINADSE333	Signal to Noise Ratio and Distortion Gain=1, Single-ended	60	—	—	dB	Fs=40 MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SINADSE333	Signal to Noise Ratio and Distortion Gain=2, Single-ended	57	—	—	dB	Fs=40 MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SINADSE333	Signal to Noise Ratio and Distortion Gain=4, Single-ended	54	—	—	dB	Fs=40 MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SINADSE333	Signal to Noise Ratio and Distortion Gain=8, Single-ended	51	—	—	dB	Fs=40 MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SINADSE333	Signal to Noise Ratio and Distortion Gain=16, Single-ended	48	—	—	dB	Fs=40 MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz.	—

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Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
						Applicable with NXP default FIR filter.	
SINADSE333_20M	Signal to Noise Ratio and Distortion Gain=1, Differential [6]	59	—	—	dB	Fs=20MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter	—
SINADSE333_20M	Signal to Noise Ratio and Distortion Gain=2, Differential [6]	57	—	—	dB	Fs=20MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter	—
SINADSE333_20M	Signal to Noise Ratio and Distortion Gain=4, Differential [6]	54	—	—	dB	Fs=20MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter	—
SINADSE333_20M	Signal to Noise Ratio and Distortion Gain=8, Differential [6]	51	—	—	dB	Fs=20MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter	—
SINADSE333_20M	Signal to Noise Ratio and Distortion Gain=16, Differential [6]	48	—	—	dB	Fs=20MHz, Output rate = 320/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter	—
SNRDIFF333	Signal to Noise Ratio GAIN=1, Differential [7]	74	—	—	dB	Fs=40 MHz, Output rate = 320ksps/ 333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—

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Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
SNRDIFF333	Signal to Noise Ratio GAIN=2, Differential [7]	71	—	—	dB	Fs=40 MHz, Output rate = 320ksps/ 333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SNRDIFF333	Signal to Noise Ratio GAIN=4, Differential [7]	68	—	—	dB	Fs=40 MHz, Output rate = 320ksps/ 333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SNRDIFF333	Signal to Noise Ratio GAIN=8, Differential [7]	65	—	—	dB	Fs=40 MHz, Output rate = 320ksps/ 333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SNRDIFF333	Signal to Noise Ratio GAIN=16, Differential [7]	62	—	—	dB	Fs=40 MHz, Output rate = 320ksps/ 333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SNRDIFF333_20M	Signal to Noise Ratio GAIN=1, Differential [6]	67	—	—	dB	Fs=20MHz, Output rate = 320ksps/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SNRDIFF333_20M	Signal to Noise Ratio GAIN=2, Differential [6]	67	—	—	dB	Fs=20MHz, Output rate = 320ksps/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—

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Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
SNRDIFF333_20M	Signal to Noise Ratio GAIN=4, Differential [6]	67	—	—	dB	Fs=20MHz, Output rate = 320ksps/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SNRDIFF333_20M	Signal to Noise Ratio GAIN=8, Differential [6]	65	—	—	dB	Fs=20MHz, Output rate = 320ksps/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SNRDIFF333_20M	Signal to Noise Ratio GAIN=16, Differential [6]	60	—	—	dB	Fs=20MHz, Output rate = 320ksps/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SINADDIFF333	Signal to Noise Ratio and Distortion Gain=1, Differential	66	—	—	dB	Fs=40 MHz, Output rate = 320ksps/ 333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SINADDIFF333	Signal to Noise Ratio and Distortion Gain=2, Differential	63	—	—	dB	Fs=40 MHz, Output rate = 320ksps/ 333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SINADDIFF333	Signal to Noise Ratio and Distortion Gain=4, Differential	60	—	—	dB	Fs=40 MHz, Output rate = 320ksps/ 333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—

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Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
SINADDIFF333	Signal to Noise Ratio and Distortion Gain=8, Differential	57	—	—	dB	Fs=40 MHz, Output rate = 320ksps/ 333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SINADDIFF333	Signal to Noise Ratio and Distortion Gain=16, Differential	54	—	—	dB	Fs=40 MHz, Output rate = 320ksps/ 333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SINADDIFF333_ 20M	Signal to Noise Ratio and Distortion Gain=1, Differential [6]	66	—	—	dB	Fs=20MHz, Output rate = 320ksps/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SINADDIFF333_ 20M	Signal to Noise Ratio and Distortion Gain=2, Differential [6]	63	—	—	dB	Fs=20MHz, Output rate = 320ksps/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SINADDIFF333_ 20M	Signal to Noise Ratio and Distortion Gain=4, Differential [6]	60	—	—	dB	Fs=20MHz, Output rate = 320ksps/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
SINADDIFF333_ 20M	Signal to Noise Ratio and Distortion Gain=8, Differential [6]	57	—	—	dB	Fs=20MHz, Output rate = 320ksps/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—

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Table 38. Sigma Delta Analog to Digital Converter (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
SINADDIFF333_20M	Signal to Noise Ratio and Distortion Gain=16, Differential [6]	54	—	—	dB	Fs=20MHz, Output rate = 320ksps/333ksps, full-scale 20kHz input, integration bandwidth up to 80/83.3kHz. Applicable with NXP default FIR filter.	—
IDDA_SDADC_BIASGEN	VDDA supply current - 1 ADC+BIASGEN	—	10.5	13.2	mA	Fs=40MHz, 1 SDADC + BIASGEN - powered ON	—
IDDA_SDADC_BIASGEN_20M	VDDA supply current - 1 ADC+BIASGEN [6]	—	9.1	11.2	mA	Fs=20MHz, 1 SDADC + BIASGEN - powered ON	—
IDDA_SDADC	VDDA supply current - 1 ADC	—	5.4	6.4	mA	Fs=40MHz, per SDADC -powered ON	—
IDDA_SDADC_20M	VDDA supply current - 1 ADC [6]	—	4.3	5	mA	Fs=20MHz, per SDADC- powered ON	—

1. When using a GAIN setting of 16, the conversion result will always have a value of zero in the least significant bit. The gives an effective resolution of 15 bits.
2. Fs=40MHz is preferred mode except for applications requiring high input impedance. Fs=20MHz mode provides higher input impedance while trading off few other specs, which are specified with condition Fs=20MHz and suffix _20M added to thier symbol names.
3. Offset and gain error due to temperature drift can occur in either direction (+/-) for each of the SDADCs on the dev
4. Conversion offset error must be divided by the applied gain factor (1, 2, 4, 8, or 16) to obtain the actual input referred offset error.
5. Calibration of gain is possible when gain = 1. Offset Calibration should be done with respect to 0.5*VDD_HV_SDADC for differential mode and single ended mode with negative input=0.5*VDD_HV_SDADC. Offset Calibration should be done with respect to 0 for "single ended mode with negative input=0". Both offset and Gain Calibration is guaranteed for ±5% variation of VDD_HV_SDADC, ±10% variation of VDD_HV_SDADC, and ± 50 °C temperature variation
6. Applicable for half sampling rate mode(Fs=20MHz).
7. Guaranteed only when input signal is between VREFP-0.15 and VREFN+0.15. Parameter observed should be normalized to full scale.

13.3 Low Power Comparator (LPCMP)

Table 39. Low Power Comparator (LPCMP)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
idda(IDHSS)	vdda Supply Current, High Speed Mode [1,2]	—	240	—	uA	—	—
idda(IDLSS)	vdda Supply Current, Low Speed Mode [1,2]	—	17	—	uA	—	—

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Table 39. Low Power Comparator (LPCMP) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
idda(IDHSS)	vdda Supply Current, high speed mode, DAC only [2]	—	10	—	uA	—	—
idda_lkg	vdda Supply Current, module disabled [2]	—	2	—	nA	vdda=5.5V, T=25C	—
TDHSB	Propagation Delay, High Speed Mode [3]	—	—	200	ns	—	—
TDLSB	Propagation Delay, Low Speed mode [3]	—	—	2	us	—	—
TDHSS	Propagation Delay, High Speed Mode [4]	—	—	400	ns	—	—
TDLSS	Propagation Delay, Low Speed mode [4]	—	—	5	us	—	—
TIDHS	Initialization Delay, High Speed Mode [5]	—	—	3	us	—	—
TIDLS	Initialization Delay, Low Speed mode [5]	—	—	30	us	—	—
VAIO	Analog Input Offset Voltage, High Speed Mode	-25	+/-1	25	mV	—	—
VAIO	Analog Input Offset Voltage, Low Speed mode	-40	+ /- 5	40	mV	—	—
VAHYST0	Analog Comparator Hysteresis, High Speed Mode	—	0	—	mV	HYSTCTR[1:0]= 2'b00	—
VAHYST1	Analog Comparator Hysteresis, High Speed Mode	—	14	41	mV	HYSTCTR[1:0]= 2'b01	—
VAHYST2	Analog Comparator Hysteresis, High Speed Mode	—	27	76	mV	HYSTCTR[1:0]= 2'b10	—
VAHYST3	Analog Comparator Hysteresis, High Speed Mode	—	40	111	mV	HYSTCTR[1:0]= 2'b11	—
VAHYST0	Analog Comparator Hysteresis, Low Speed mode	—	0	—	mV	HYSTCTR[1:0]= 2'b00	—

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Table 39. Low Power Comparator (LPCMP) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VAHYST1	Analog Comparator Hysteresis, Low Speed mode	—	8	60	mV	HYSTCTR[1:0]= 2'b01	—
VAHYST2	Analog Comparator Hysteresis, Low Speed mode	—	15	113	mV	HYSTCTR[1:0]= 2'b10	—
VAHYST3	Analog Comparator Hysteresis, Low Speed mode	—	23	165	mV	HYSTCTR[1:0]= 2'b11	—
INL	DAC integral linearity [2,6,7]	-1	—	1	LSB	vrefh_cmp = vdda, vrefl_cmp = vss	—
INL	DAC integral linearity [2,6,7]	-1.5	—	1.5	LSB	vrefh_cmp < vdda	—
DNL	DAC differential linearity [2,6]	-1	—	1	LSB	vrefh_cmp = vdda, vrefl_cmp = vss	—
DNL	DAC differential linearity [2,6]	-1.5	—	1.5	LSB	vrefh_cmp < vdda	—
tDDAC	DAC Initialization time	—	—	30	us	—	—
VAIN	Analog input voltage	0	—	VDDA	V	—	—

1. Difference at input > 200mV
2. vdda is comparator HV supply and internally shorted to VDD_HV_A pin. vss is comparator ground
3. Applied +/- (100 mV + VAHYST0/1/2/3 + max. of VAIO) around switch point
4. Applied +/- (30 mV + VAHYST0/1/2/3 + max. of VAIO) around switch point
5. Applied ± (100 mV + VAHYST0/1/2/3).
6. 1 LSB = (vrefh_cmp - vrefl_cmp) /256. vrefh_cmp and vrefl_cmp are comparator reference high and low
7. Calculation method used: Linear Regression Least Square Method

LPCMP0 channels must only be selected/enabled when VDD_HV_A >= VDD_HV_B. These channels must be disabled when VDD_HV_A goes below VDD_HV_B.

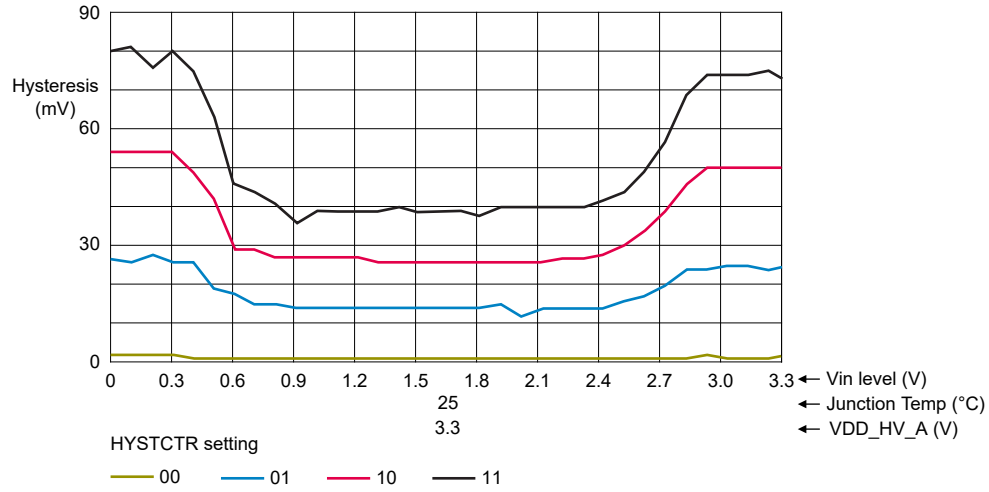

Figure 17. Typical Hysteresis vs Vin level (VDD_HV_A = 3.3 V, High Speed Mode)

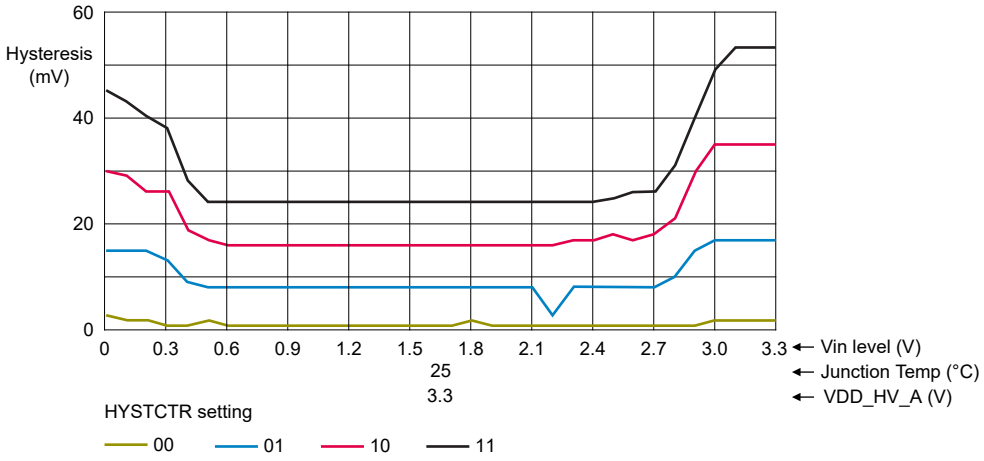

Figure 18. Typical Hysteresis vs Vin level (VDD_HV_A = 3.3 V, Low Speed Mode)

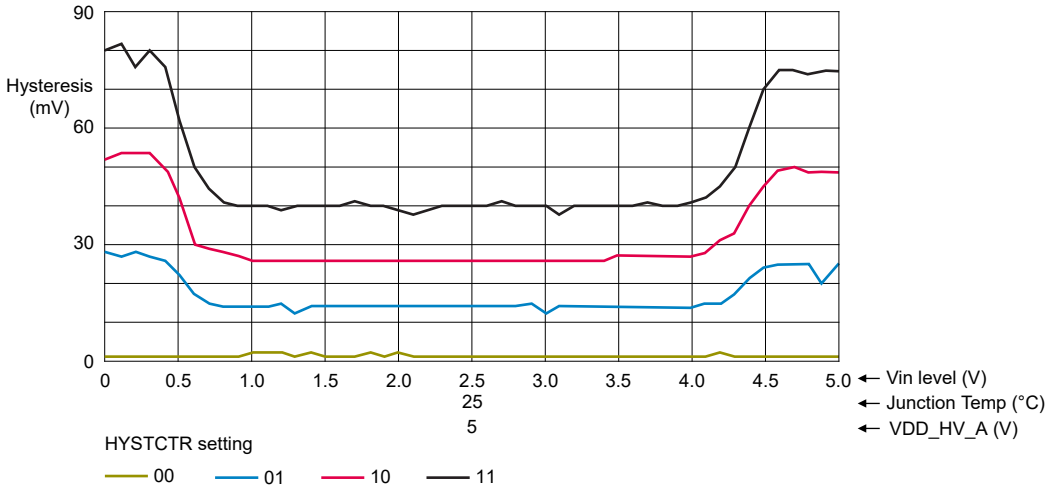

Figure 19. Typical Hysteresis vs Vin level (VDD_HV_A = 5 V, High Speed Mode).png

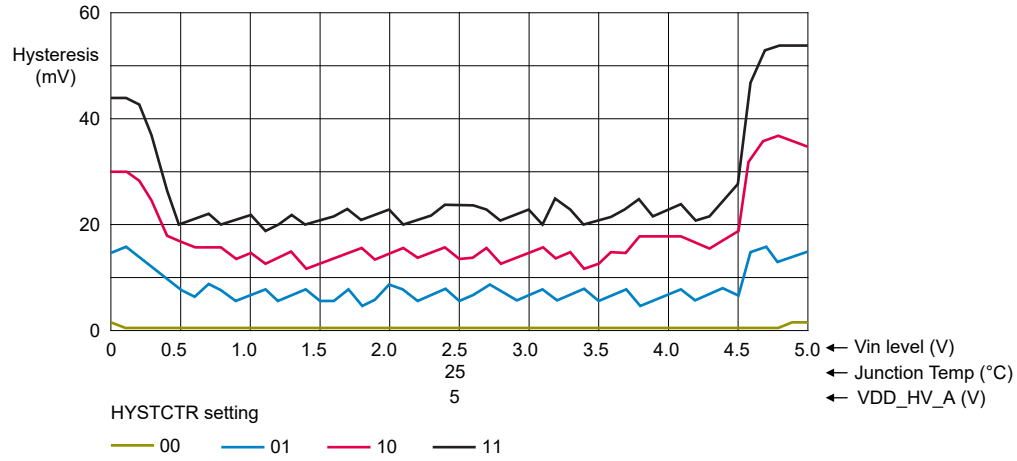

Figure 20. Typical Hysteresis vs Vin level (VDD_HV_A = 5 V, Low Speed Mode).png

13.4 Sine wave generator

Table 40. Sine wave generator

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
INPUT_CLK	Input clock	12	16	20	MHz	—	—
APP	Sine wave amplitude [1]	0.394	—	2.302	V	—	—
MAXAPP	Maximum amplitude (pk-pk) [2]	1.884	2.093	2.302	V	—	—
MINAPP	Minimum amplitude (pk-pk) [2]	0.394	0.438	0.482	V	—	—
AV	Amplitude Variation [3]	-10	—	10	%	—	—
CV	Common voltage [4]	—	1.3	—	V	—	—
CVV	Common voltage variation	-6	—	6	%	—	—
SINAD	Signal to noise ratio plus distortion [5]	30	45	—	dB	—	—
FREQ	Frequency range of the sine wave	1	—	50	kHz	—	—
FRP	Frequency precision of the sine wave (peak to peak variation)	-5	—	5	%	—	—
Cload	Load capacitance	25	—	100	pF	—	—
Resd	ESD Pad Resistance [6]	149	213	277	ohm	—	—
Iout	Output current	0	—	100	uA	—	—

1. Peak to peak value is measured with no R or I load and its range is for room temperature
2. Peak-to-peak value is measured with no R or I load
3. Peak to peak excludes noise, SINAD must be considered.
4. Common mode value is measured with no R or I load
5. SINAD is measured at Max Peak-to-Peak voltage. SINAD may not be met with FIRC clock source.
6. Internal device routing resistance. ESD pad resistance is in series and must be considered for Max peak to peak voltages, depending on application I load and/or R load

13.5 Supply Diagnosis

The table below gives the specification for the on die supply diagnosis.

Table 41. Supply Diagnosis

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
AN_ACC	Offset to internally monitored supply at ADC input [1,2,3]	-5	0	5	%	—	—
AN_T_on	Switching time from closed (OFF) to conducting (ON) [1]	—	2.5	12	ns	—	—
AN_TADCSA	Required ADC sampling time [2]	1.2	—	—	µs	—	—

1. These specs will have degraded performance when used in extended supply voltage operation range, i.e. normal supply voltage range specification is exceeded.
2. Required ADC sampling time specified by parameter AN_TADCSA needs to be used at the ADC conversion to guarantee the specified accuracy. A smaller sampling time leads to a less accurate result.
3. If V15 > VDD_HV_A +100mV then the V15 measurement via anamux may be imprecise.

13.6 Temperature Sensor

The table below gives the specification for the MCU on-die temperature sensor.

Table 42. Temperature Sensor

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TS_TJ	Junction temperature monitoring range	-40	—	150	°C	—	—
TS_IV25	ON state current consumption on V25	—	400	—	µA	ETS_EN=1	—
TS_ACC1	Temperature output error at circuit output (Voltage) [1,2,3]	-5	0	+5	°C	100 °C < Tj <= 150 °C	—
TS_ACC2	Temperature output error at circuit output (Voltage) [1,2,3]	-10	0	+10	°C	-40 °C <= Tj <=100 °C	—
TS_TSTART	Circuit start up time	—	4	30	µs	—	—
TS_TADCSA	Required ADC sampling time [1]	1.2	—	—	µs	—	—

1. Required ADC sampling time specified by parameter TS_TADCSA needs to be used at the ADC conversion to guarantee the specified accuracy. A smaller sampling time leads to a less accurate result.
2. Note: The temperature sensor measures the junction temperature Tj at the location where it is placed on die. The local Tj is modulated by current and previous active state of the circuit elements on die.
3. The error caused by ADC conversion and provided temperature calculation formula is not included.

14 Clocking modules

14.1 Fast External Oscillator (FXOSC)

Table 43. Fast External Oscillator (FXOSC)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FREQ_BYPASS	Input clock frequency in bypass mode [1]	—	—	50	MHz	—	—
TRF_BYPASS	Input clock rise/fall time in bypass mode [1]	—	—	5	ns	—	—
CLKIN_DUTY_BYPASS	Input clock duty cycle in bypass mode [1]	47.5	—	52.5	%	—	—
FXOSC_CLK	output clock frequency in crystal mode	8	—	40	MHz	—	—
TFXOSC	Fxosc start up time (ALC enabled) [2]	—	—	2	ms	—	—
IFXOSC	Oscillator Analog circuit supply current, V25 supply (ALC enable)	—	—	1	mA	using 8, 16 or 40 MHz crystal	—
IFXOSC	Oscillator Analog circuit supply current, V25 supply (ALC disabled)	—	—	2.7	mA	using 8, 16 or 40 MHz crystal	—
EXTAL_SWING_PP	Peak-to-peak voltage swing on EXTAL pin in crystal oscillator mode (ALC enabled)	0.3	—	1.4	V	—	—
EXTAL_SWING_PP	Peak-to-peak voltage swing on EXTAL pin in crystal oscillator mode (ALC disabled) [3]	1.2	—	2.75	V	—	—
CLKIN_VIL_EXTAL_BYPASS	Input clock low level in bypass mode	0	—	vref-0.5	V	vref=0.5*VDD_HV_A	—

Table continues on the next page...

Table 43. Fast External Oscillator (FXOSC) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
CLKIN_VIH_EXTAL_BYPASS	Input clock high level in bypass mode	vref+0.5	—	VDD_HV_A	V	vref=0.5*VDD_HV_A	—
VSB	Self Bias Voltage	350	—	850	mV	—	—
GM	Amplifier Transconductance	9.7	—	18.5	mA/V	GM_SEL[3:0] = 4`b1111	—

1. For bypass mode applications, the EXTAL pin should be driven low when FXOSC is in off/disabled state.
2. The startup time specification is valid only when the recommended crystal and load capacitors are used. For higher load capacitances, the actual startup time might be higher.
3. The recommended gm setting to ensure extal swing < 2.75V at 8MHz in ALC-disabled mode is gm=4'b0010. Recommended gm settings in ALC-disabled mode for all other supported frequencies and crystals remain the same.

To ensure stable oscillations, FXOSC incorporates the feedback resistance internally.

Drive level is a crystal specification and if crystal load capacitance is increased beyond the recommended value, it may violate the crystal drive level rating. In such cases, contact NXP sales representative for selecting the correct crystal.

Crystal oscillator circuit provides stable oscillations when gmXOSC > 5 * gm_crit. The gm_crit is defined as:

$gm\_crit = 4 * (ESR + RS) * (2\pi F)^2 * (C0 + CL)^2$

where:

- gmXOSC is the transconductance of the internal oscillator circuit
- ESR is the equivalent series resistance of the external crystal
- RS is the series resistance connected between XTAL pin and external crystal for current limitation
- F is the external crystal oscillation frequency
- C0 is the shunt capacitance of the external crystal
- CL is the external crystal total load capacitance. CL = Cs+ [C1*C2/(C1+C2)]
- Cs is stray or parasitic capacitance on the pin due to any PCB traces
- C1, C2 external load capacitances on EXTAL and XTAL pins

See manufacture datasheet for external crystal component values

Figure 21. Oscillation build-up equation

NOTE

To improve the FXOSC & PLL jitter performance, following pins(PTG0,PTG2,PTG3,PTG6,PTF29, PMOS_CTRL in BGA289 package) cannot be toggling edge-aligned.

NOTE

For 176LQFP, To improve FXOSC jitter with SMPS ON use VDD_DCDC=3.3 V.

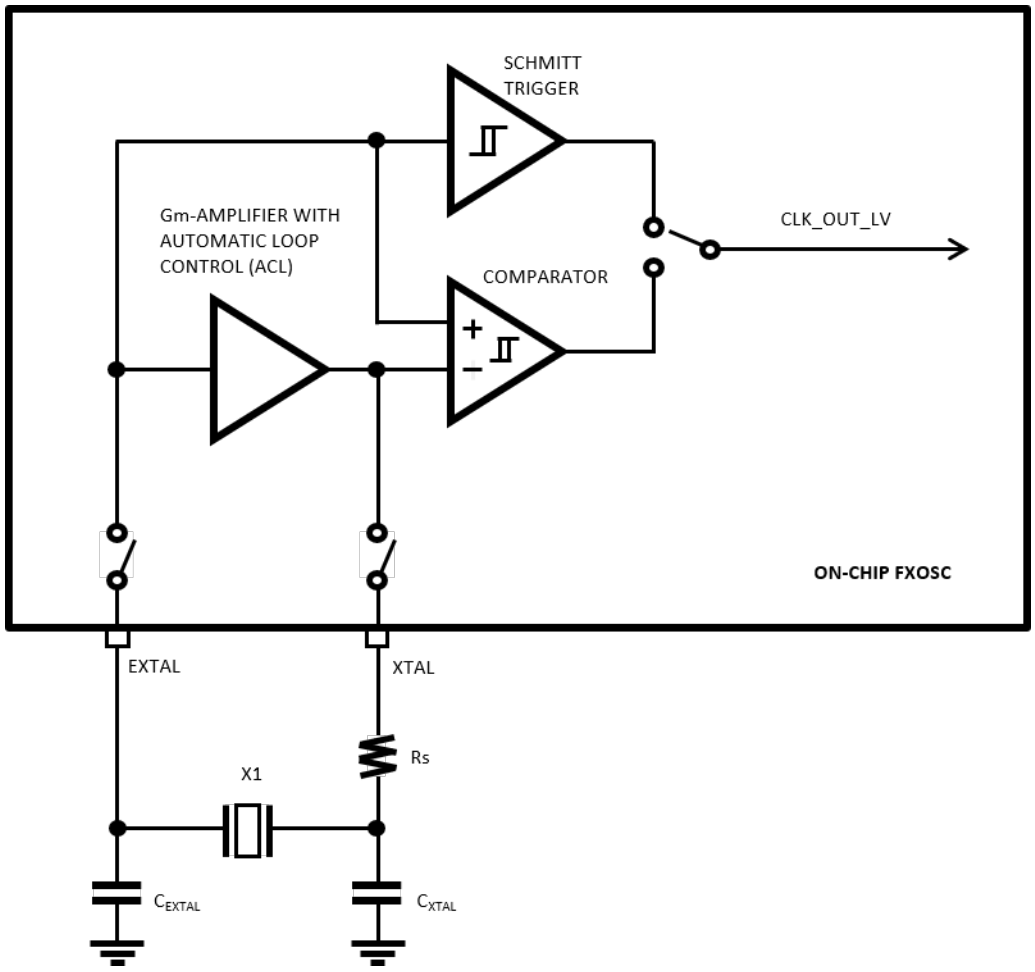

Figure 22. Block diagram

14.2 FIRC

Table 44. FIRC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fFIRC	FIRC nominal Frequency	—	48	—	MHz	—	—
FACC	FIRC Frequency deviation across process, voltage, and temperature after trimming	-5	—	5	%	—	—
TSTART	Startup Time [1]	—	10	25	us	—	—

1. Startup time is for reference only.

14.3 SIRC

Table 45. SIRC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSIRC	SIRC nominal Frequency	—	32	—	KHz	—	—
fSIRC_ACC	SIRC Frequency deviation across process, voltage, and temperature after trimming	-10	—	10	%	—	—
TSIRC_start	SIRC Startup Time [1]	—	—	3	ms	—	—
TSIRC_DC	SIRC duty cycle	30	—	70	%	—	—

1. Startup time is for information only.

14.4 PLL

Jitter values specified in this table are applicable for FXOSC reference clock input only.

Table 46. PLL

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FPLL_in	PLL input frequency	8	—	40	MHz	This is the frequency after the Reference Divider within the PLL	—
FPLL_out	PLL output frequency (PLL_PHIn_CLK)	48	—	480	MHz	—	—
FPLL_vcoRange	VCO Frequency range	640	—	960	MHz	—	—
FPLL_DS	Modulation Depth (down spread)	-0.5	—	-3	%	—	—
FPLL_FM	Modulation frequency	—	—	32	KHz	—	—
TPLL_start	PLL lock time	—	—	1	ms	—	—
JPLL_cyc	PLL period jitter (pk-pk) [1,2,3]	—	—	208	ps	FPLL_out = 320MHz, Integer Mode	—
JPLL_cyc	PLL period jitter (pk-pk) [1,2,3]	—	—	395	ps	FPLL_out = 320MHz, Fractional Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [1,2,3]	—	—	840	ps	FPLL_out = 320MHz, Integer Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [1,2,3]	—	—	1680	ps	FPLL_out = 320MHz, Fractional Mode	—

Table continues on the next page...

Table 46. PLL (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
JPLL_cyc	PLL period jitter (pk-pk) [1,2,3]	—	—	237	ps	FPLL_out = 240MHz, Integer Mode	—
JPLL_cyc	PLL period jitter (pk-pk) [1,2,3]	—	—	487	ps	FPLL_out = 240MHz, Fractional Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [1,2,3]	—	—	840	ps	FPLL_out = 240MHz, Integer Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [1,2,3]	—	—	1680	ps	FPLL_out = 240MHz, Fractional Mode	—
JPLL_cyc	PLL period jitter (pk-pk) [1,2,3]	—	—	295	ps	FPLL_out = 160MHz, Integer Mode	—
JPLL_cyc	PLL period jitter (pk-pk) [1,2,3]	—	—	670	ps	FPLL_out = 160MHz, Fractional Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [1,2,3]	—	—	840	ps	FPLL_out = 160MHz, Integer Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [1,2,3]	—	—	1680	ps	FPLL_out = 160MHz, Fractional Mode	—
JPLL_cyc	PLL period jitter (pk-pk) [1,2,3]	—	—	353	ps	FPLL_out = 120MHz, Integer Mode	—
JPLL_cyc	PLL period jitter (pk-pk) [1,2,3]	—	—	853	ps	FPLL_out = 120MHz, Fractional Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [1,2,3]	—	—	840	ps	FPLL_out = 120MHz, Integer Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [1,2,3]	—	—	1680	ps	FPLL_out = 120MHz, Fractional Mode	—

1. For SSCG, jitter due to systematic modulation needs to be added as per applied modulation. Accumulated jitter specification is not valid with SSCG
2. Jitter numbers are valid only at IP boundary and does not include any degradation due to IO pad for clock measurement.
3. Jitter numbers calculated by extrapolating RMS jitter numbers to +/- 7 sigma .

15 Communication interfaces

15.1 LPSPI

15.1.1 LPSPI

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following table provides timing characteristics for classic LPSPI timing modes.

1.All timing is shown with respect to 50% VDD_HV_A/B thresholds.

2. All measurements are with maximum output load of 30pF, input transition of 1 ns and pad configured DSE = 1, SRC = 0

Table 47. LPSPI

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fperiph	Peripheral Frequency [1,2,3]	—	—	40	MHz	Master	—
fperiph	Peripheral Frequency [1,2,3]	—	—	40	MHz	Slave	—
fperiph	Peripheral Frequency [1,3,4]	—	—	80	MHz	Master Loopback	—
fop	Operating frequency	—	—	15	MHz	Slave	1
fop	Operating frequency	—	—	15	MHz	Master	1
fop	Operating frequency [5]	—	—	10	MHz	Slave_10Mbps	1
fop	Operating frequency [5]	—	—	10	MHz	Master_10Mbps	1
fop	Operating frequency [4,6]	—	—	20	MHz	Master Loopback	1
tSPSCK	SPSCK period	66	—	—	ns	Slave	2
tSPSCK	SPSCK period	66	—	—	ns	Master	2
tSPSCK	SPSCK period [4]	50	—	—	ns	Master Loopback	2
tSPSCK	SPSCK period	100	—	—	ns	Master_10Mbps	2
tSPSCK	SPSCK period	100	—	—	ns	Slave_10Mbps	2
tLEAD	Enable lead time (PCS to SPSCK delay) [7]	tSPCK/2	—	—	ns	Slave	3
tLEAD	Enable lead time (PCS to SPSCK delay) [7]	30	—	—	ns	Master	3
tLEAD	Enable lead time (PCS to SPSCK delay) [4,7]	30	—	—	ns	Master Loopback	3
tLAG	Enable lag time (After SPSCK delay) [8]	tSPCK/2	—	—	ns	Slave	4
tLAG	Enable lag time (After SPSCK delay) [8]	30	—	—	ns	Master	4
tLAG	Enable lag time (After SPSCK delay) [4,8]	30	—	—	ns	Master Loopback	4

Table continues on the next page...

Table 47. LPSPI (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tWSPCK	Clock (SPSCK) time (SPSCK duty cycle) [9]	tSPSCK/2 - 3	—	tSPSCK/2 + 3	ns	Slave	5
tWSPCK	Clock (SPSCK) time (SPSCK duty cycle) [9]	tSPSCK/2 - 3	—	tSPSCK/2 + 3	ns	Master	5
tWSPCK	Clock (SPSCK) time (SPSCK duty cycle) [4,9]	tSPSCK/2 - 3	—	tSPSCK/2 + 3	ns	Master Loopback	5
tSU	Data setup time(inputs)	6	—	—	ns	Slave	6
tSU	Data setup time(inputs)	25	—	—	ns	Master	6
tSU	Data setup time(inputs)	5	—	—	ns	Slave_10Mbps	6
tSU	Data setup time(inputs)	36	—	—	ns	Master_10Mbps	6
tSU	Data setup time(inputs) [4]	6	—	—	ns	Master_Loopback	6
tHI	Data hold time(inputs)	3	—	—	ns	Slave	7
tHI	Data hold time(inputs)	0	—	—	ns	Master	7
tHI	Data hold time(inputs)	4	—	—	ns	Slave_10Mbps	7
tHI	Data hold time(inputs)	0	—	—	ns	Master_10Mbps	7
tHI	Data hold time(inputs) [4]	3	—	—	ns	Master Loopback	7
tA	Slave access time	—	—	50	ns	Slave	8
tDIS	Slave MISO (SOUT) disable time	—	—	50	ns	Slave	9
tV	Data valid (after SPSCK edge) [10]	—	—	26	ns	Slave	10
tV	Data valid (after SPSCK edge) [10]	—	—	14	ns	Master	10
tV	Data valid (after SPSCK edge) [10]	—	—	41	ns	Slave_10Mbps	10

Table continues on the next page...

Table 47. LPSPI (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tV	Data valid (after SPSCK edge) [10]	—	—	21	ns	Master_10Mbps	10
tV	Data valid (after SPSCK edge) [4,10]	—	—	17.5	ns	Master Loopback	10
tHO	Data hold time (outputs) [10]	3	—	—	ns	Slave	11
tHO	Data hold time (outputs) [10]	-8	—	—	ns	Master	11
tHO	Data hold time (outputs) [10]	3	—	—	ns	Slave_10Mbps	11
tHO	Data hold time (outputs) [10]	-15	—	—	ns	Master_10Mbps	11
tHO	Data hold time (outputs) [4,10]	-2	—	—	ns	Master Loopback	11
tRI/FI	Rise/Fall time input [11]	—	—	1	ns	Slave	-
tRI/FI	Rise/Fall time input [11]	—	—	1	ns	Master	-
tRI/FI	Rise/Fall time input [4,11]	—	—	1	ns	Master Loopback	-

1. tperiph = 1/fperiph
2. For LPSPI0 instance, max. peripheral frequency is equal to AIPS_PLAT_CLK.
3. fperiph = LPSPI peripheral clock
4. Master Loopback mode: In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1.
5. These specifications apply to the SPI operation, as master or slave, at up to 10 Mbps for the combinations not indicated in the table below. Unless otherwise noted, all other ‘master’ and ‘slave’ specifications are also applicable in the 10Mbps configurations. See table "LPSPI 20 MHz and 15 MHz Combinations.
6. LPSPI0 support up to 20MHz on fast pin.
7. Minimum configuration value for CCR[PCSSCK] field is 3(0x00000011).
8. Minimum configuration value for CCR[SCKPCS] field is 3(0x00000011).
9. While selecting odd dividers, ensure Duty Cycle is meeting this parameter.
10. Output rise/fall time is determined by the output load and GPIO pad drive strength setting. See the GPIO specifications for detail.
11. The input rise/fall time specification applies to both clock and data, and is required to guarantee related timing parameters.

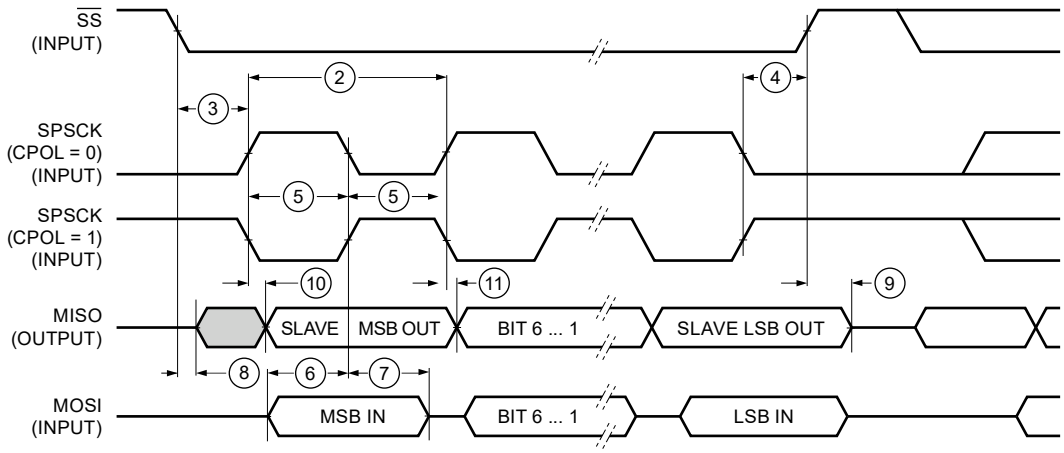

Figure 23. LPSPI Slave Mode Timing (CPHA=1)

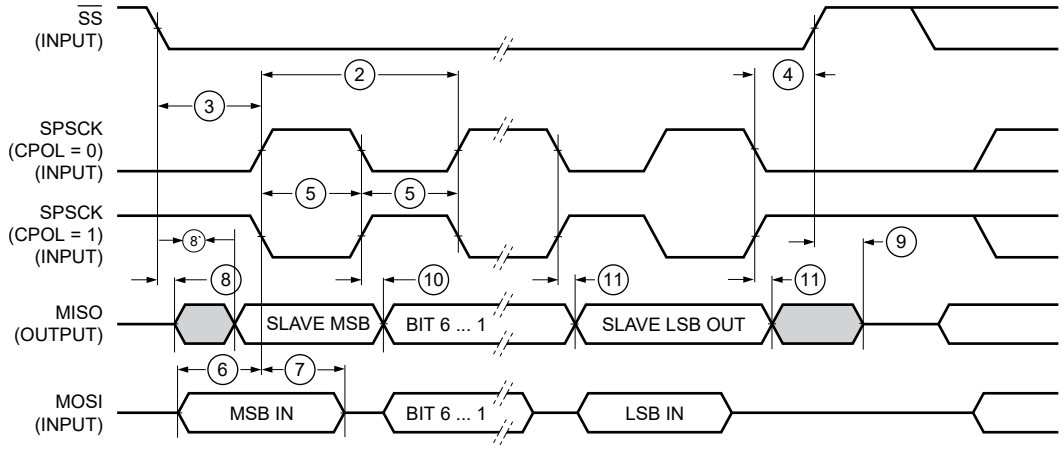

Figure 24. LPSPI Slave Mode Timing (CPHA=0)

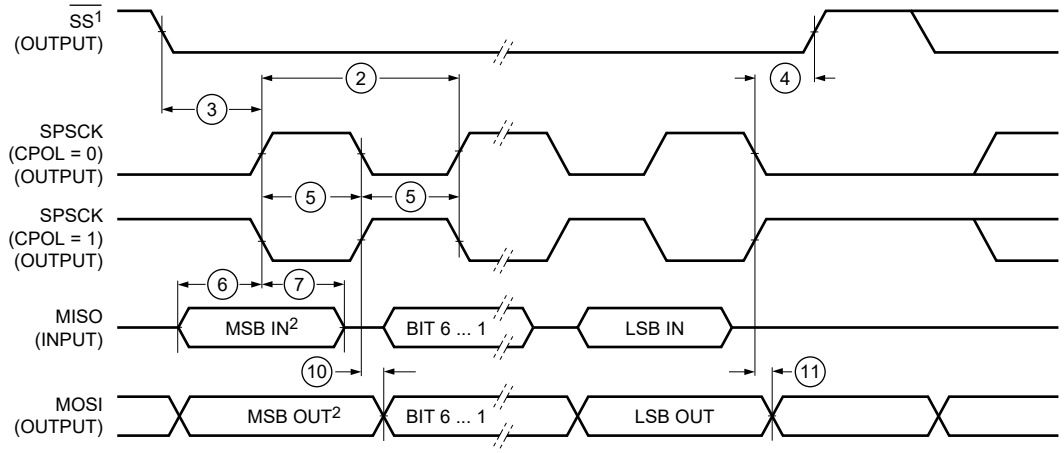

Figure 25. LPSPI Master Mode Timing (CPHA=0)

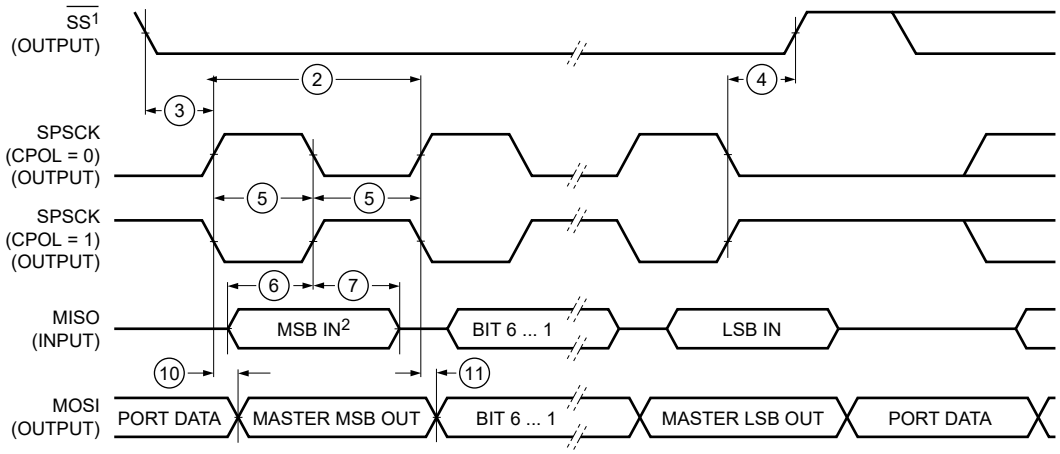

Figure 26. LPSPI Master Mode Timing (CPHA=1)

15.1.2 LPSPI0 20 MHz and 15 MHz Combinations

NOTE

All measurements are with maximum output load of 25pF

Table 48. LPSPI0 20 MHz and 15 MHz Combinations

PORT	PAD TYPE	SPI Signal	20Mbps (In loopback mode only)	15 Mbps
PTB1	GPIO-Slow	LPSPI0_SOUT		LPSPI0_SOUT
PTB0	GPIO-Slow	LPSPI0_PCS0		LPSPI0_PCS0
PTC9	GPIO-Slow	LPSPI0_SIN		LPSPI0_SIN
PTC8	GPIO-Slow	LPSPI0_SCK		LPSPI0_SCK
PTD6	GPIO-Medium	LPSPI0_PCS0	LPSPI0_PCS0	
PTD5	GPIO-Medium	LPSPI0_PCS1	LPSPI0_PCS1	
PTD12	GPIO-FAST	LPSPI0_SOUT	LPSPI0_SOUT	
PTD11	GPIO-FAST	LPSPI0_SCK	LPSPI0_SCK	
PTD10	GPIO-FAST	LPSPI0_SIN	LPSPI0_SIN	

NOTE

Trace length should not exceed 11 inches for SCK pad when used in Master loopback mode.

15.1.3 LPSPI Pad Type

Timing is not supported for below combination of Clock (FAST) and DATA(Super-Slow)

Table 49. LPSPI Pad Type

SPI Clock	Fast PadPort	SPI Data	Superslow Pad Port
LPSPI0_SCK	PTD11	LPSPI0_SIN	PTE0

Table continues on the next page...

Table 49. LPSPI Pad Type (continued)

SPI Clock	Fast PadPort	SPI Data	Superslow Pad Port
			PTD16
		LPSPI0_PCS0	PTA26
			PTE4
		LPSPI0_PCS4	PTD23
		LPSPI0_PCS5	PTD24
		LPSPI0_PCS6	PTD20
		LPSPI0_PCS7	PTD21
LPSPI2_SCK	PTB29	LPSPI2_SIN	PTE16
			PTF1
		LPSPI2_SOUT	PTA8
			PTF2
		LPSPI2_PCS0	PTA9
			PTE11
			PTF3
		LPSPI2_PCS1	PTE10
		LPSPI2_PCS2	PTA21
		LPSPI2_PCS3	PTF26
			PTE26
LPSPI3_SCK	PTC17	LPSPI3_SIN	PTE10
			PTD20
			PTF12
		LPSPI3_SOUT	PTD0
			PTA17
			PTF15
		LPSPI3_PCS0	PTD17
			PTB17
			PTA9
			PTF16
		LPSPI3_PCS1	PTF18
			PTA6
		LPSPI3_PCS2	PTB13
			PTF19

Table continues on the next page...

Table 49. LPSPI Pad Type (continued)

SPI Clock	Fast PadPort	SPI Data	Superslow Pad Port
		LPSPI3_PCS3	PTB12
			PTF23

15.2 MDIO timing specifications

The following table describes the MDIO electrical characteristics. Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1 and SRE = 1’b0). I/O operating voltage ranges from 2.97 V to 3.63 V. MDIO pin must have external Pull-up.

Table 50. MDIO timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	MDC clock frequency	—	—	2.5	MHz	—	—
MDC1	MDC pulse width high	40	—	60	%MDC period	—	MDC1
MDC2	MDC pulse width low	40	—	60	%MDC period	—	MDC2
MDC5	MDC falling edge to MDIO output valid(maximum propagation delay)	—	—	25	ns	—	MDC5
MDC6	MDC falling edge to MDIO output invalid(minimum propagation delay)	-10	—	—	ns	—	MDC6
MDC3	MDIO (input) to MDC rising edge setup time	28	—	—	ns	—	MDC3
MDC4	MDIO (input) to MDC rising edge hold time	0	—	—	ns	—	MDC4

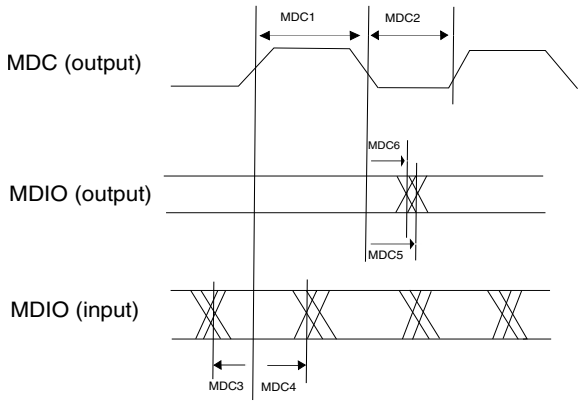

Figure 27. MII/RMII serial management channel timing

15.3 Ethernet MII (10/100 Mbps)

The following timing specs are defined at the device I/O pin and must be translated appropriately to arrive at timing specs/ constraints for the physical interface. Measurements are with maximum output load of 25pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97 V to 3.63 V.

NOTE

QuadSPI cannot be used along with Ethernet in 176LQFP-EP.

Table 51. Ethernet MII (10/100 Mbps)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	RXCLK frequency	—	2.5/25	—	MHz	10/100 Mbps	—
MII1	RXCLK pulse width high	35	—	65	%RXCLK period	—	—
MII2	RXCLK pulse width low	35	—	65	%RXCLK period	—	—
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	—	ns	10/100 Mbps	—
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	—	ns	10/100 Mbps	—
tCYC_TX	TXCLK frequency	—	2.5 / 25	—	MHz	10/100 Mbps	—
MII5	TXCLK pulse width high	35	—	65	%TXCLK period	—	—
MII6	TXCLK pulse width low	35	—	65	%TXCLK period	—	—
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	—	ns	—	—
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	—	25	ns	—	—

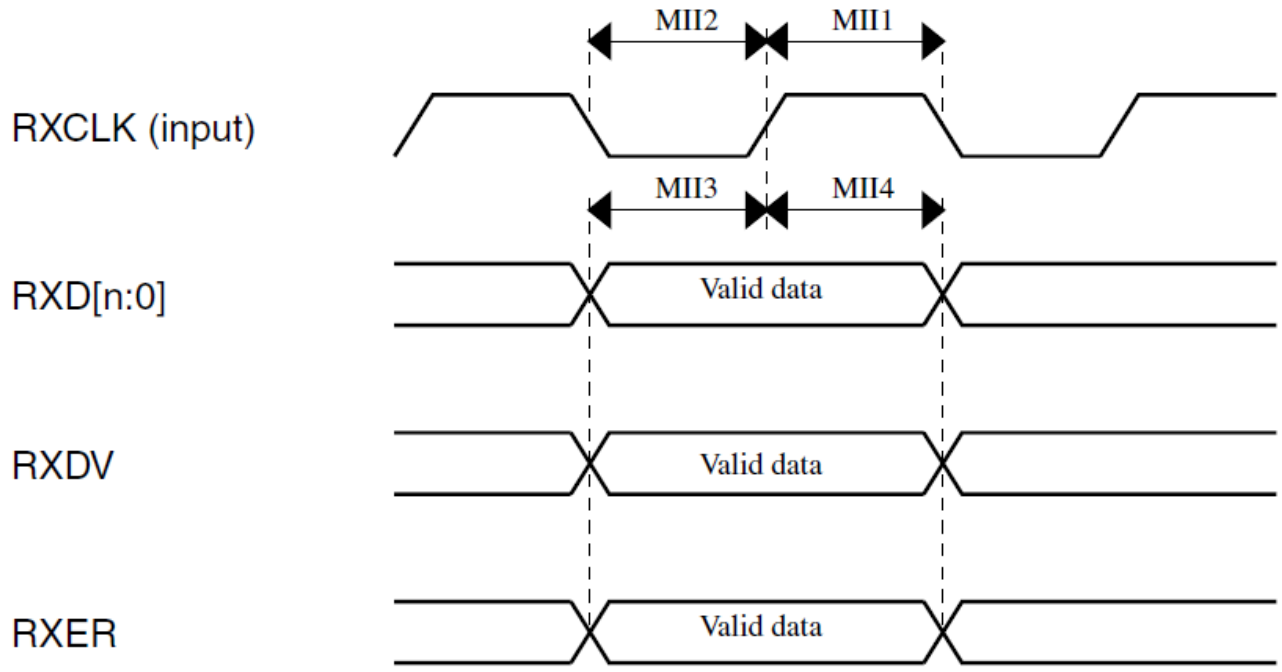

Figure 28. MII receive diagram

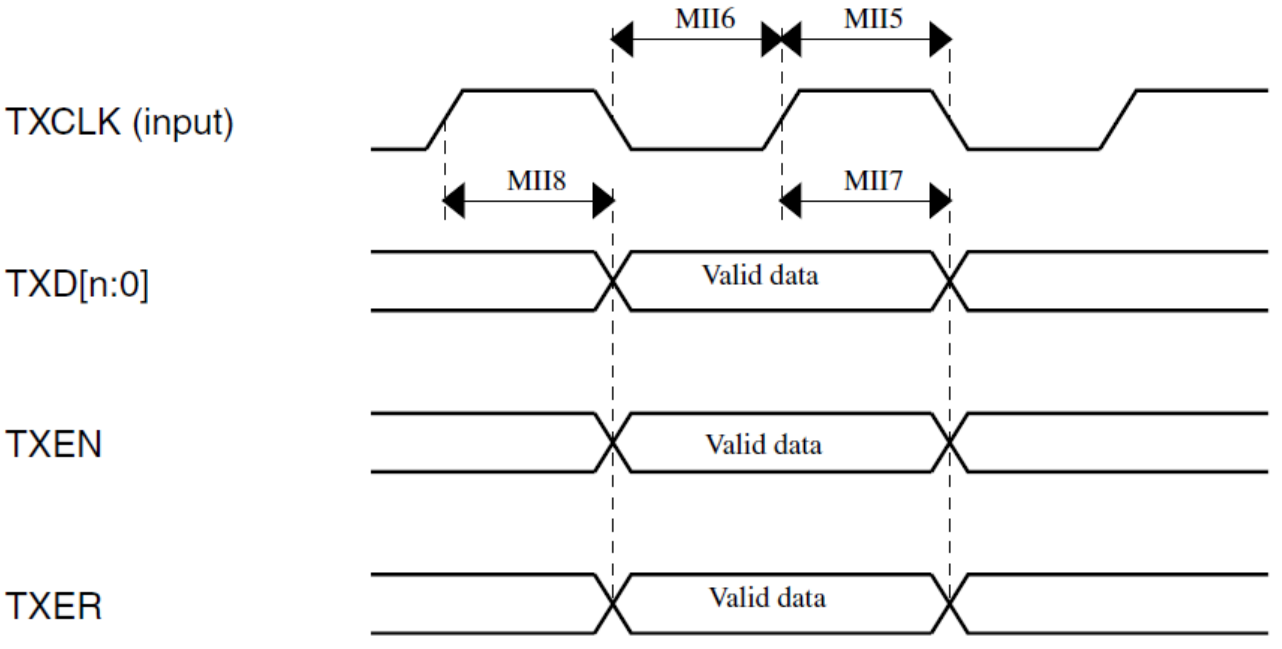

Figure 29. MII transmit diagram

15.4 Ethernet MII (200 Mbps)

The following timing specs are defined at the device I/O pin and must be translated appropriately to arrive at timing specs/ constraints for the physical interface. Measurements are with maximum output load of 25pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97 V to 3.63 V.

NOTE

QuadSPI cannot be used along with Ethernet in 176LQFP-EP

Table 52. Ethernet MII (200 Mbps)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	RXCLK frequency	—	—	50	MHz	—	—
MII1	RXCLK pulse width high	35	—	65	% RXCLK period	—	—
MII2	RXCLK pulse width low	35	—	65	% RXCLK period	—	—
MII3	RXD[3:0], RXDV, RXER to RXCLK setup time	4	—	—	ns	—	—
MII4	RXCLK to RXD[3:0], RXDV, RXER hold time	2	—	—	ns	—	—
—	TXCLK frequency	—	—	50	MHz	—	—
MII5	TXCLK pulse width high	35	—	65	% TXCLK period	—	—
MII6	TXCLK pulse width low	35	—	65	% TXCLK period	—	—
MII7	TXCLK to TXD[3:0], TXDV, TXER invalid	2	—	—	ns	—	—
MII8	TXCLK to TXD[3:0], TXDV, TXER valid	—	—	15	ns	—	—

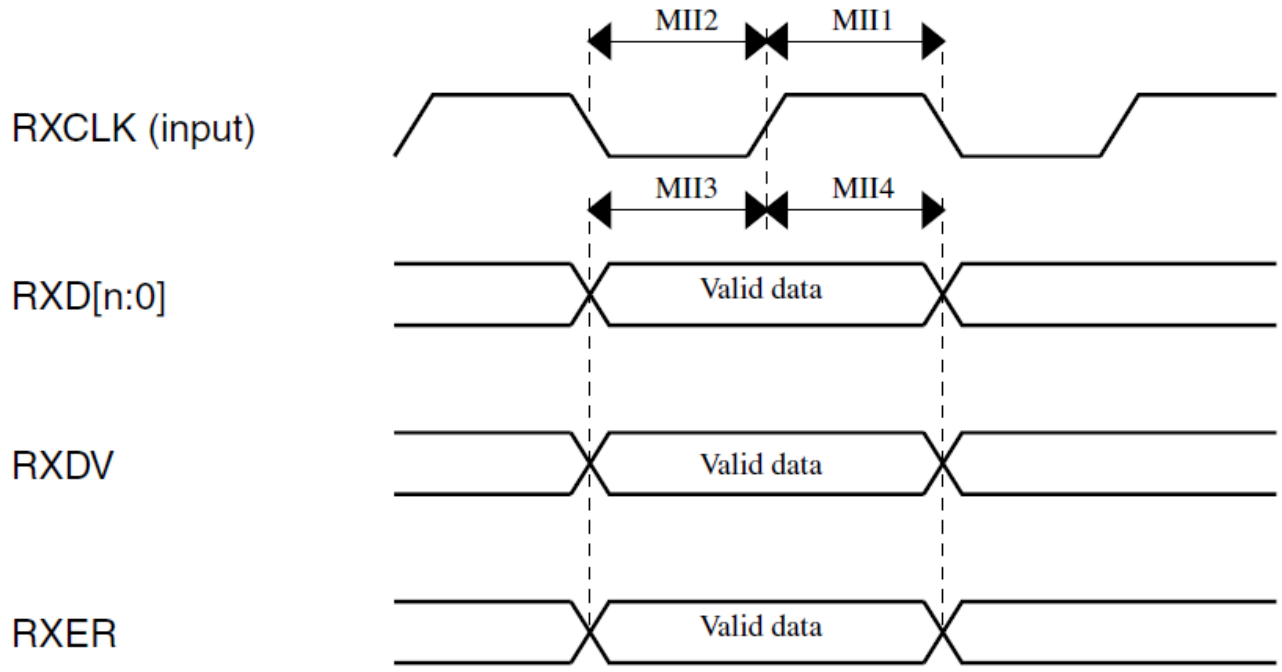

Figure 30. MII receive diagram

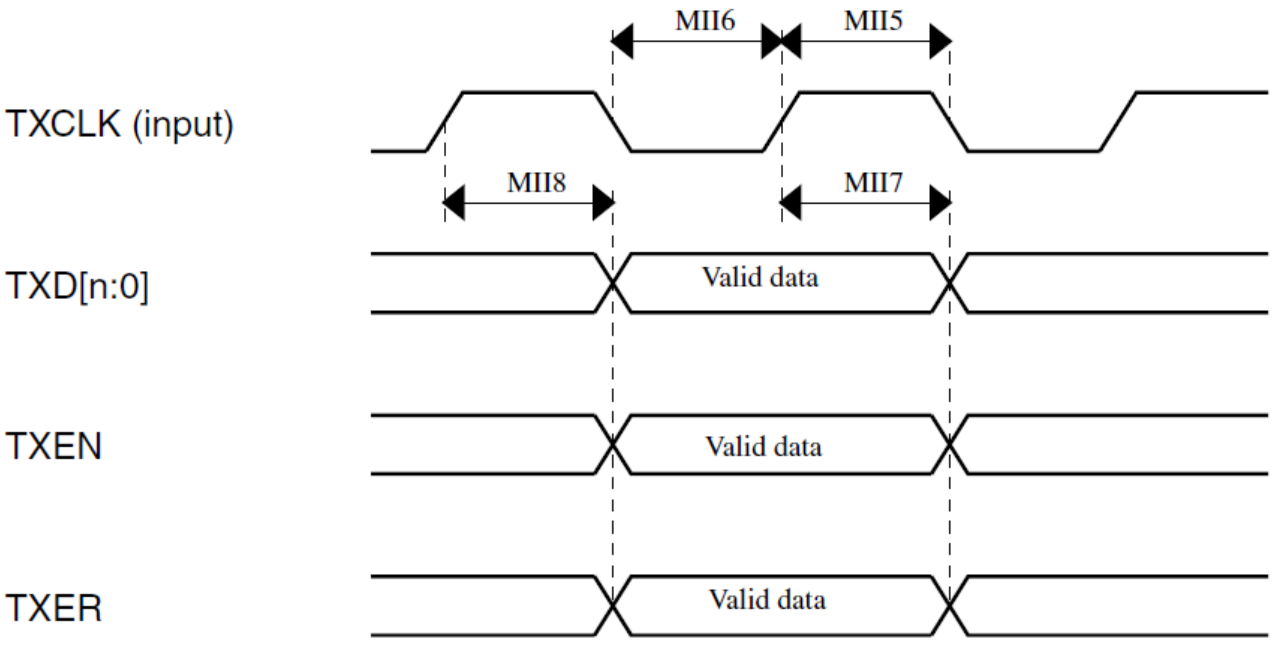

Figure 31. MII transmit diagram

15.5 Ethernet RMII (10/100 Mbps)

The following timing specs are defined at the device I/O pin and must be translated appropriately to arrive at timing specs/ constraints for the physical interface. Measurements are with maximum output load of 25pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97 V to 3.63 V.

NOTE

QuadSPI cannot be used along with Ethernet in 176LQFP-EP

Table 53. Ethernet RMII (10/100 Mbps)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	RMII input clock frequency (RMII_CLK)	—	—	50	MHz	10/100 Mbps	—
RMII1,RMII5	RMII_CLK pulse width high	35	—	65	%RMII_CLK period	—	—
RMII2,RMII6	RMII_CLK pulse width low	35	—	65	%RMII_CLK period	—	—
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	—	ns	—	—
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	—	ns	—	—
RMII8	RMII_CLK to TXD[1:0], TXEN data valid	—	—	15	ns	—	—
RMII7	RMII_CLK to TXD[1:0], TXEN data invalid	2	—	—	ns	—	—

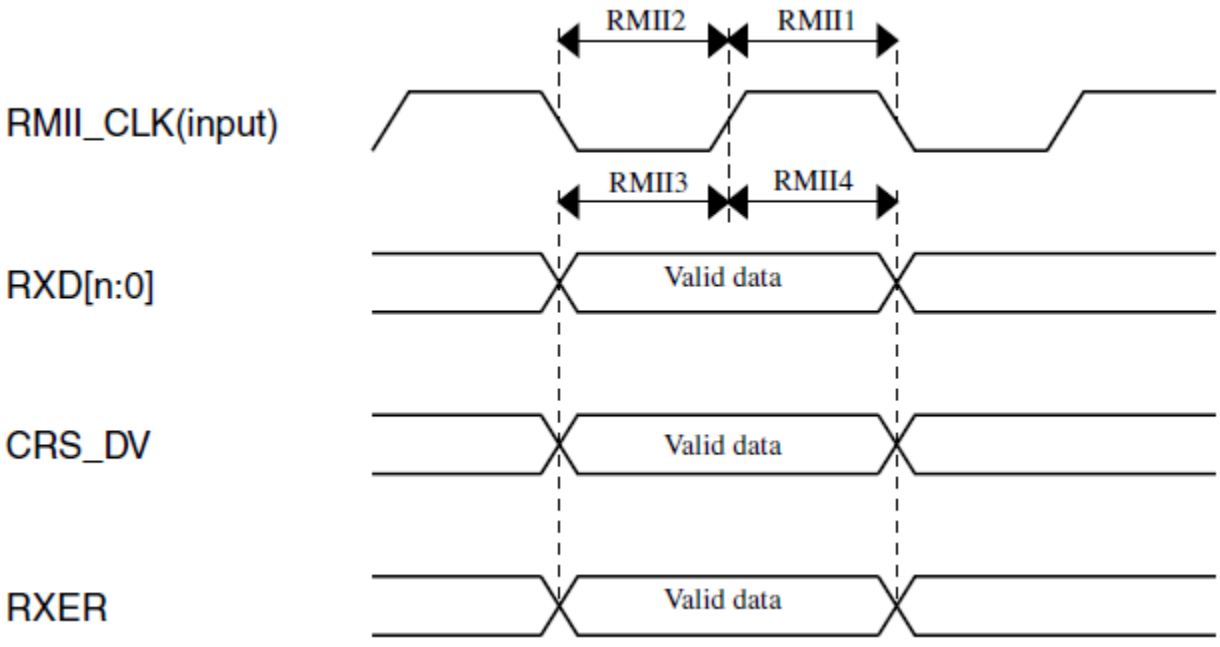

Figure 32. RMII receive diagram

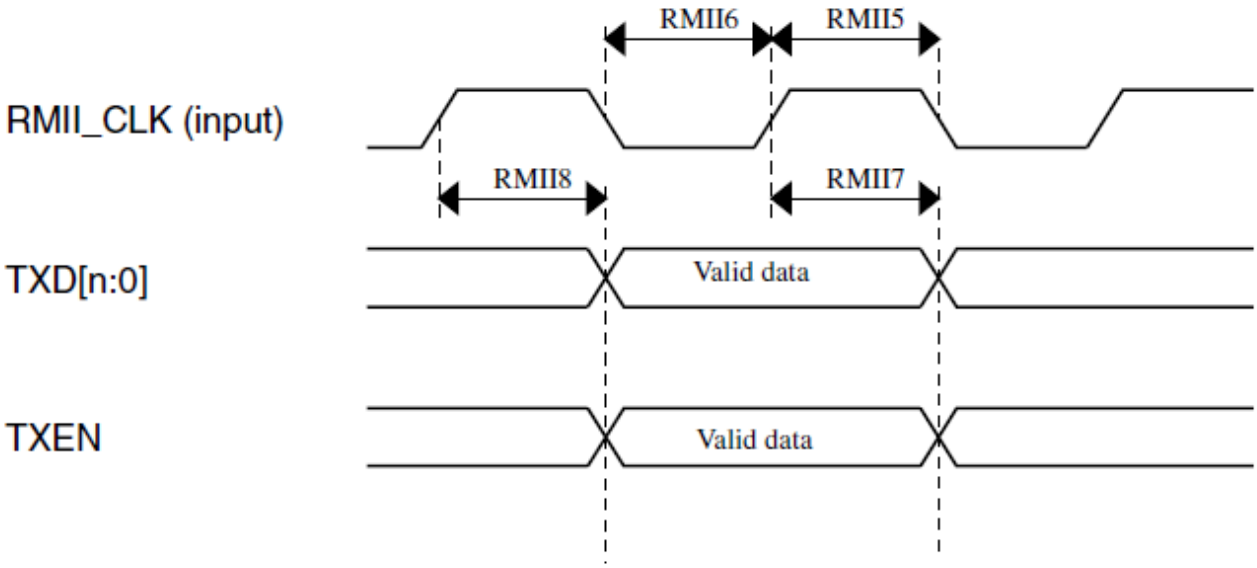

Figure 33. RMII transmit diagram

15.6 I2C

See I/O parameters for I^2C specification.

15.7 FlexCAN characteristics

See I/O parameters for FlexCAN specification.

15.8 LPUART characteristics

See I/O parameters for LPUART specification.

15.9 SPI

NOTE

This module corresponds with DSPI section in RM

DRE=1 & SRE=0 is the required drive setting to meet the timing.

Table 54. SPI

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSCK	SPI cycle time [1,2]	100	—	10000	ns	Master, MTFE=0	—
tCSC	PCS to SCK delay [3]	20	—	10000	ns	—	2
tASC	After SCK delay [4]	20	—	10000	ns	—	3
tSDC	SCK duty cycle	40	—	60	%	—	4
tPCSC	PCSx to PCSS time	13	—	—	ns	—	7
tPASC	PCSS to PCSx time	13	—	—	ns	—	8
tSUI	Input data setup time [5,6]	27	—	—	ns	Master, MTFE=0	—
tHI	Input data hold time [5]	0	—	—	ns	Master, MTFE=0	10
tSUO	Output data valid time (after SCK edge) [7]	—	—	5	ns	—	—
tHO	Output data hold time [7]	-2	—	—	ns	—	—

1. SMPL_PTR should be set to 1. For SPI_CTARn[BR] - 'Baud Rate Scaler' configuration is >= 3
2. The maximum SPI baud rate that is achievable in a dedicated master-slave connection depends on several parameters that are independent of the SPI module clocking capabilities (e.g. capacitive load of the signal lines, SPI slave clock-to-data delay, pad slew rate, etc.). The maximum achievable SPI baud rate needs to be evaluated in a corresponding SPI master-slave setup.
3. This value of 20 ns is with the configuration prescaler values: SPI_CTARn[PCSSCK] - "PCS to SCK Delay Prescaler" configuration is "3" (01h) and SPI_CTARn[CSSCK] - "PCS to SCK Delay Scaler" configuration is "2" (0000h)
4. This value of 20 ns is with the configuration prescaler values: SPI_CTARn[PASC] - "After SCK Delay Prescaler" configuration is "3" (01h) and SPI_CTARn[ASC] - "After SCK Delay Scaler" configuration is "2" (0000h)
5. Input timing assumes an input signal slew rate of 2ns (20%/80%).
6. For the case of both master and slave being NXP S32x devices, frequency of operation will be reduced to [1000 /2* {tSUI_master + tSUO_slave + PCB delay}] in ns.
7. Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).

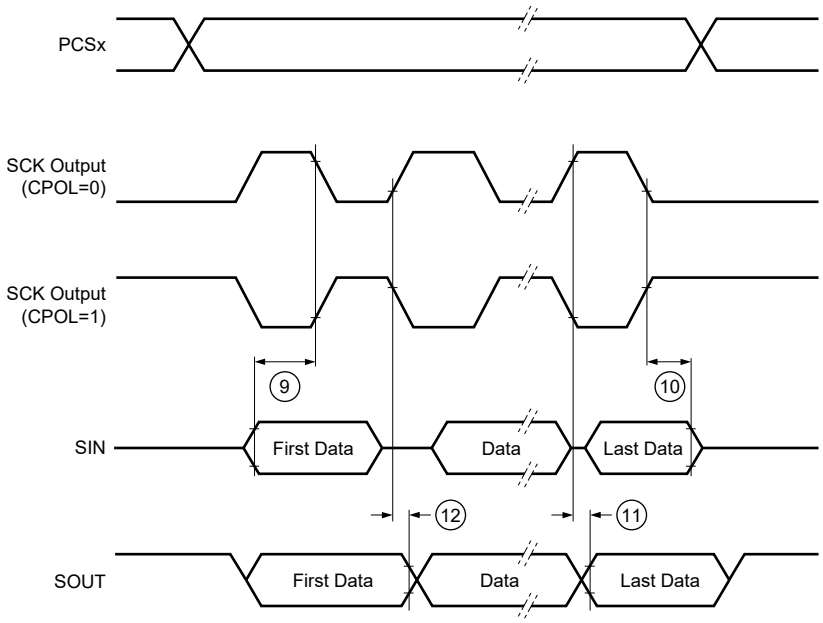

Figure 34. SPI Classic Timing - Master, CPHA = 1, MTFE=0

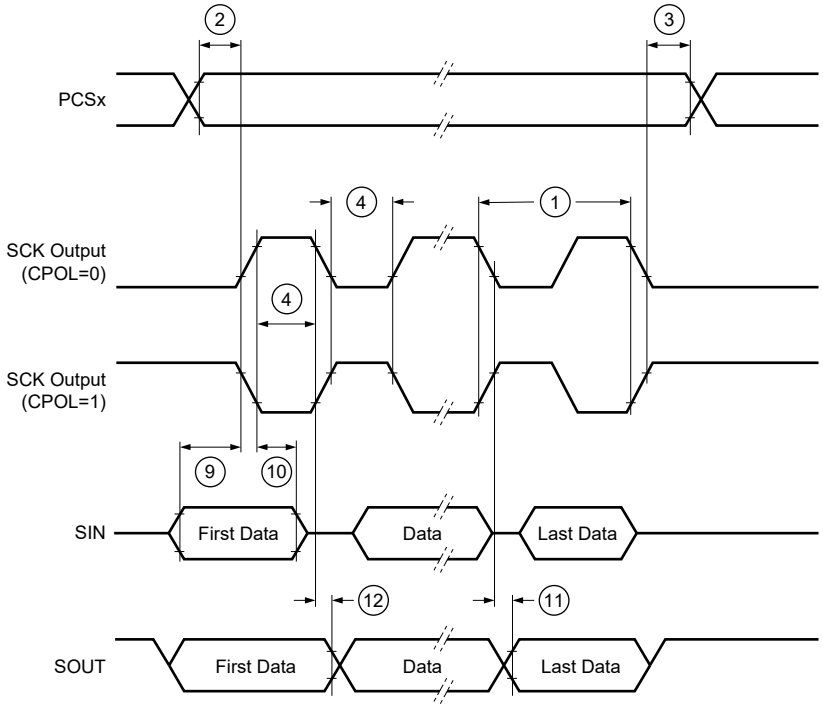

Figure 35. SPI Classic Timing - Master, CPHA = 0, MTFE=0

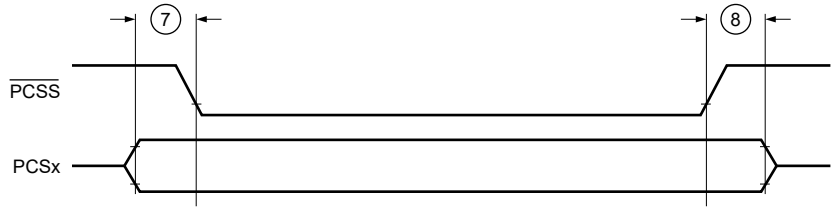

Figure 36. SPI PCS Strobe (PCSS) Timing

15.10 Microsecond channel (MSC)

These specs apply to both LVDS and GPIO.

NOTE

This module corresponds with DSPI in RM.

Table 55. Microsecond channel (MSC)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSCK	MSC-LVDS cycle time	25	—	—	ns	LVDS	1
tSCK	MSC-GPIO cycle time [1]	40	—	—	ns	GPIO	1
tCSV	PCS valid after SCK [2]	—	—	26	ns	GPIO	—
tCSH	PCS hold after SCK [2]	-4	—	—	ns	—	—
tSUO	Output data valid time (after SCK edge)	—	—	5	ns	—	11
tHO	Output data hold time	-2	—	—	ns	—	12
t1	Duty cycle deviation	-1	—	1	ns	—	—
t2	Rise time	0.4	—	7	ns	ZL=100R, CL<50, 40 MHz	—
t2	Rise time	0.4	—	4	ns	ZL=100R, CL<25, 100 MHz	—
t3	Fall time	0.4	—	7	ns	ZL=100R, CL<50, 40 MHz	—
t3	Fall time	0.4	—	4	ns	ZL=100R, CL<25, 100 MHz	—

1. If MSC functionality is not used it can be used as SPI interface
2. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of SPI_CLKn. This timing value is due to pad delays and signal propagation delays.

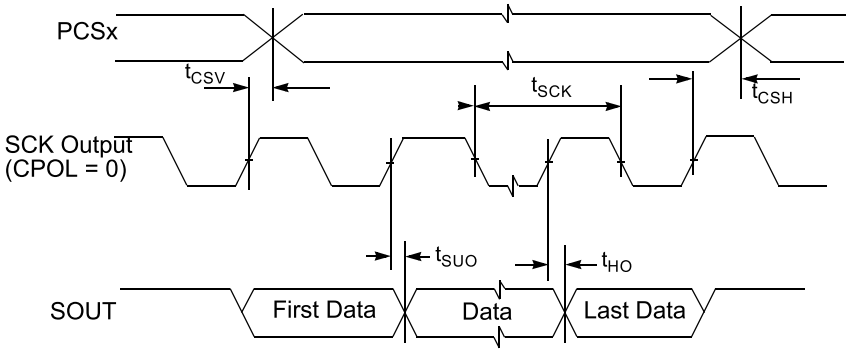

Figure 37. SPI ,aster timing, output only

15.11 Zipwire

See LVDS 3.3V Receiver/Transmitter Electrical Specifications for Zipwire specification.

15.12 LFAST PLL

Table 56. LFAST PLL

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fPLL_CLKIN	PLL Input Clock Frequency	10	—	26	MHz	—	—
DCREF	PLL Input Reference Clock Duty Cycle	45	—	55	%	—	—
ΔPERREF	PLL Input Reference Clock Jitter	-100	—	100	ps	long term, up to 10MHz, fRF_REF = 20MHz	—
fLFAST_CLK	PLL Output Clock Frequency Range	320	—	480	MHz	—	—
tLOCK	PLL Lock Time	—	—	250	us	fRF_REF = 20MHz	—
PER_jitter	PLL Period Jitter (RMS)	—	—	40	ps	fRF_REF = 20MHz	—
RJ	PLL Long Term Random Jitter	—	50	—	ps	VCO clock measured over 100us acquisition at ZipWire Tx LVDS across 100ohm load.	—
DJ	PLL Long Term Deterministic Jitter [1]	—	80	500	ps	VCO clock measured over 100us acquisition at ZipWire Tx LVDS across 100ohm load.	—
TOT_jitter	Total Jitter	—	1.09	1.31	ns	BER = 10-9	—

Table continues on the next page...

Table 56. LFAST PLL (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IPLL_HV	PLL HV Supply Current Consumption	—	—	5	mA	fPLL_VCO = 960MHz	—
IPLL_LV	PLL LV Supply Current Consumption	—	—	5	mA	fPLL_VCO = 960MHz	—

1. DJ max jitter includes influence of edge aligned IO activity

16 Memory interfaces

16.1 QuadSPI Octal 3.3V DDR 120MHz

The following table describes the QuadSPI electrical characteristics. Measurements are with maximum output load of 25pF, input transition of 1ns and pads configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97V to 3.63V. QuadSPI trace length should be less than or equal to 2 inches. For Single and Dual IO modes of operation if external device doesn't have pull-up feature, then external pull-up must be added at board level for unused device pins. With external pull-up, performance of the interface may degrade in Quad IO mode based on load associated with external pull-up. QuadSPI support delay chain upto length 16, wherein delay length of low-frequency segment is 16 and length of high-frequency segment is 0. See the device Reference Manual for register and bit descriptions.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply

Table 57. QuadSPI Octal 3.3V DDR 120MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK_DQS	SCK / DQS frequency [1]	—	—	120	MHz	DLL enabled	—
fSCK_DQS	SCK / DQS frequency [1]	—	—	120	MHz	DLL mode enabled	—
tSCK	SCK clock period	1/ fSCK_DQS	—	—	ns	External DQS	—
tSDC	SCK / DQS duty cycle	45	—	55	%	External DQS	—
tCL_SCK_DQS	SCK / DQS low time [1]	3.75	—	—	ns	—	—
tCH_SCK_DQS	SCK / DQS high time [1]	3.75	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK)	0.816	—	2.934	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK)	3.016	—	-0.766	ns	—	—

Table continues on the next page...

Table 57. QuadSPI Octal 3.3V DDR 120MHz (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tISU_DQS	Input setup time (w.r.t. DQS) [1]	-0.616	—	—	ns	—	—
tIH_DQS	Input hold time (w.r.t. DQS) [1]	3.134	—	—	ns	—	—

1. Input timing assumes an input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.

16.2 QuadSPI Quad 3.3V SDR 120MHz

The following table describes the QuadSPI electrical characteristics. Measurements are with maximum output load of 25pF, input transition of 1ns and pads configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97V to 3.63V. QuadSPI trace length should be less than or equal to 2 inches. For Single and Dual IO modes of operation if external device doesn't have pull-up feature, then external pull-up must be added at board level for unused device pins. With external pull-up, performance of the interface may degrade in Quad IO mode based on load associated with external pull-up. QuadSPI support delay chain upto length 16, wherein delay length of low-frequency segment is 16 and length of high-frequency segment is 0. See the device Reference Manual for register and bit descriptions.

Program register value QuadSPI_FLSHCR[TCSS] = 4`h3.

Program register value QuadSPI_FLSHCR[TCSH] = 4`h3.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 58. QuadSPI Quad 3.3V SDR 120MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency [1]	—	—	120	MHz	Pad Loopback	—
tSCK	SCK clock period	1/fSCK	—	—	ns	Pad Loopback	—
tSDC	SCK duty cycle	45	—	55	%	Pad Loopback	—
tIS	Data input setup time	2	—	—	ns	Pad Loopback	—
tIH	Data input hold time	1	—	—	ns	Pad Loopback	—
tOV	Data output valid time	—	—	1.75	ns	Pad Loopback	—
tIV	Data output invalid time	-1.5	—	—	ns	Pad Loopback	—
tCSSCK	CS to SCK time	5	—	—	ns	Pad Loopback	—
tSCKCS	SCK to CS time	3	—	—	ns	Pad Loopback	—
tDVW	Input data valid window	4.62	—	—	ns	—	—

1. This frequency specification is valid only if output valid time of external flash is ≤ 5.5ns, and if output valid time of external flash is more than 5.5ns but ≤ 6.5ns, then maximum fSCK is 104MHz.

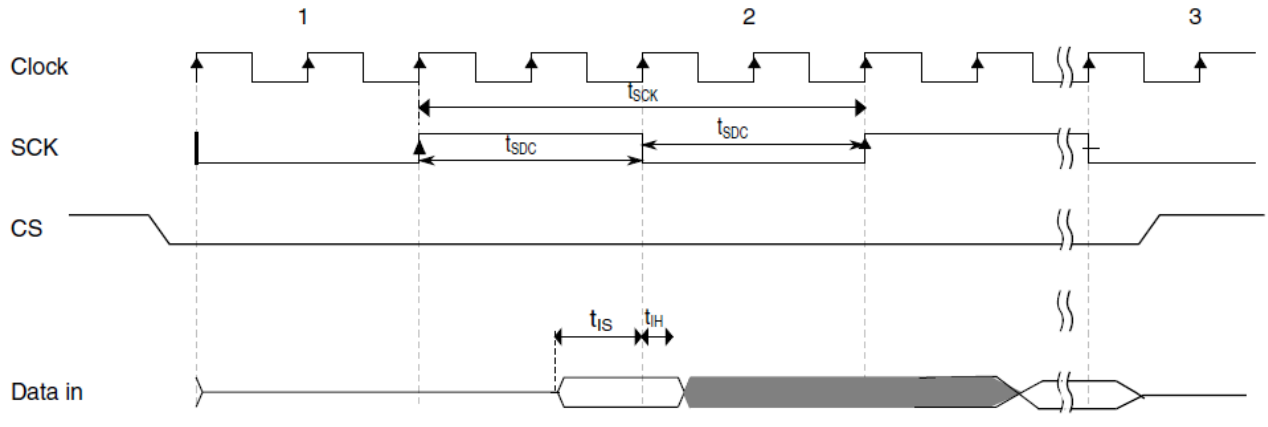

Figure 38. QuadSPI input timing (SDR mode)

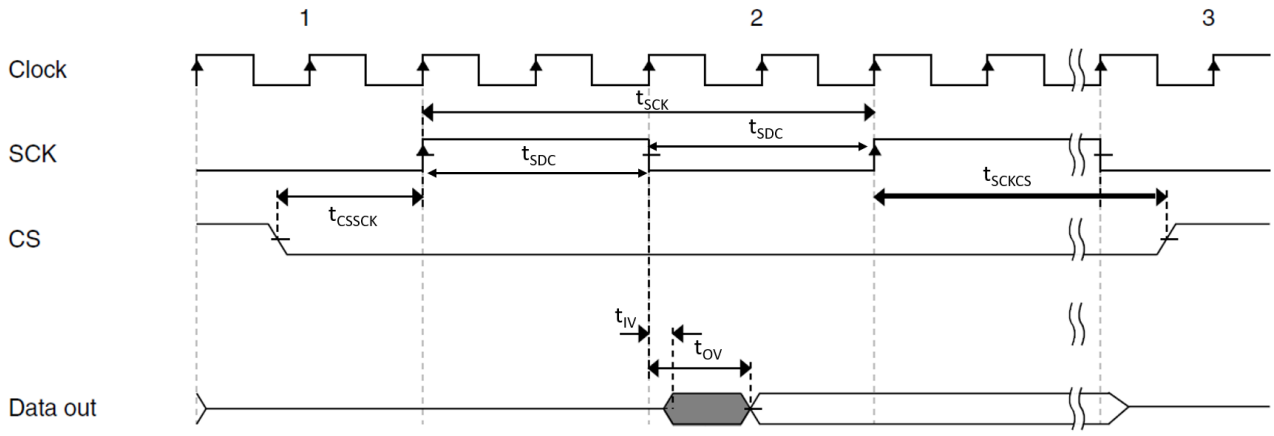

Figure 39. QuadSPI output timing (SDR mode)

16.3 QuadSPI configurations

Table 59. QuadSPI configurations (120 DDR)

Parameter	Value
Frequency	120 MHz
DDR/SDR	DDR
External DQS alignment	Edge-aligned
Flash type	Octal Flash
FLSHCR[TDH]	1
FLSHCR[TCHS]	3
FLSHCR[TCSS]	3
MCR[DLPEN]	1

Table continues on the next page...

Table 59. QuadSPI configurations (120 DDR) (continued)

Parameter	Value
DLLCR[DLLEN]	1
DLLCR[FREQEN]	0
DLLCR[DLL_REFCNTR]	2
DLLCR[DLLRES]	8
DLLCR[SLV_FINE_OFFSET]	0
DLLCR[SLV_DLY_OFFSET]	0
DLLCR (SLV_DLY_COARSE]	NA
DLLCR[SLV_DLY_FINE]	NA
DLLCR[SLAVE_AUTO_UPDT]	1
DLLCR[SLV_EN]	1
DLLCR[SLV_DLL_BYPASS]	0
DLLCR[SLV_UPD][1]	
SMPR[DLLFSMPF*]	4
SMPR[FSDLY]	0
SMPR[FSPHS]	NA

1. See Chapter "DLL and delay chain usage" for the DLLCR programming sequence

Table 60. QuadSPI configurations (120 SDR)

Parameter	Value
Frequency	120 MHz
DDR/SDR	SDR
External DQS alignment	Internal DQS Dummy pad loopback
Flash type	Quad
FLSHCR[TDH]	NA
FLSHCR[TCHS]	3
FLSHCR[TCSS]	3
MCR[DLPEN]	0
DLLCR[DLLEN]	0
DLLCR[FREQEN]	0
DLLCR[DLL_REFCNTR]	NA
DLLCR[DLLRES]	NA
DLLCR[SLV_FINE_OFFSET]	0
DLLCR[SLV_DLY_OFFSET]	0

Table continues on the next page...

Table 60. QuadSPI configurations (120 SDR) (continued)

Parameter	Value
DLLCR (SLV_DLY_COARSE]	0
DLLCR[SLV_DLY_FINE]	0
DLLCR[SLAVE_AUTO_UPDT]	0
DLLCR[SLV_EN]	1
DLLCR[SLV_DLL_BYPASS]	1
DLLCR[SLV_UPD][1]	
SMPR[DLLFSMPF*]	0
SMPR[FSDLY]	0
SMPR[FSPHS]	1

17 Debug modules

17.1 Debug trace timing specifications

The following table describes the Debug trace electrical characteristics. Measurements are with maximum output load of 25pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0.

Table 61. Debug trace timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fTRACE	Trace clock frequency (trace on Fast pads)	—	—	120	MHz	—	—
fTRACE	Trace clock frequency (trace on StandardPlus pads)	—	—	25	MHz	—	—
tDVW	Data output valid window	1.2	—	—	ns	—	—
tDIV	Data output invalid	0.3	—	—	ns	—	—

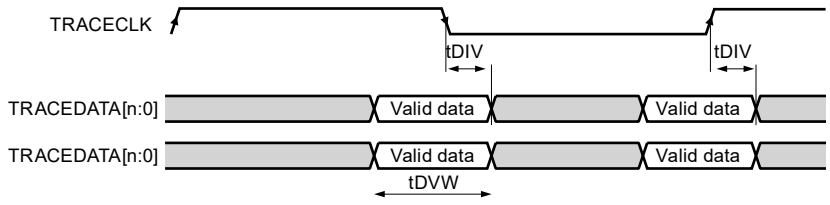

Figure 40. Trace CLKOUT specifications

17.2 JTAG electrical specifications

The following table describes the JTAG electrical characteristics. These specifications apply to JTAG and boundary scan. Measurements are with maximum output load of 30pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0.

Table 62. JTAG electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tJCYC	TCK cycle time [1,2]	30	—	—	ns	—	1
tJDC	TCK clock pulse width	40	—	60	%	—	2
tTCKRISE	TCK rise/fall times (40%-70%)	—	—	1	ns	—	3
tTMSS, tTDIS	TMS, TDI data setup time	5	—	—	ns	—	4
tTMSH, tTDIH	TMS, TDI data hold time	5	—	—	ns	—	5
tTDOV	TCK low to TDO data valid [3]	—	—	22	ns	—	6
tTDOI	TCK low to TDO data invalid	0	—	—	ns	—	7
tTDOHZ	TCK low to TDO high impedance	—	—	22	ns	—	8
tBSDV	TCK falling edge to output valid [4]	—	—	600	ns	—	11
tBSDVZ	TCK falling edge to output valid out of high impedance	—	—	600	ns	—	12
tBSDHZ	TCK falling edge to output high impedance	—	—	600	ns	—	13
tBSDST	Boundary scan input valid to TCK rising edge	15	—	—	ns	—	14
tBSDHT	TCK rising edge to boundary scan input invalid	15	—	—	ns	—	15

1. Cycle time is 30ns assuming full cycle timing. Cycle time is 60ns assuming half cycle timing.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

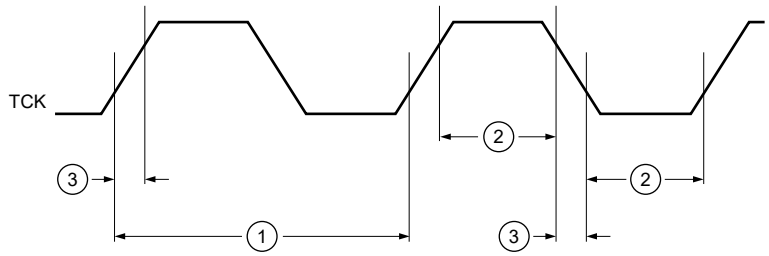

Figure 41. JTAG TCK Input Timing

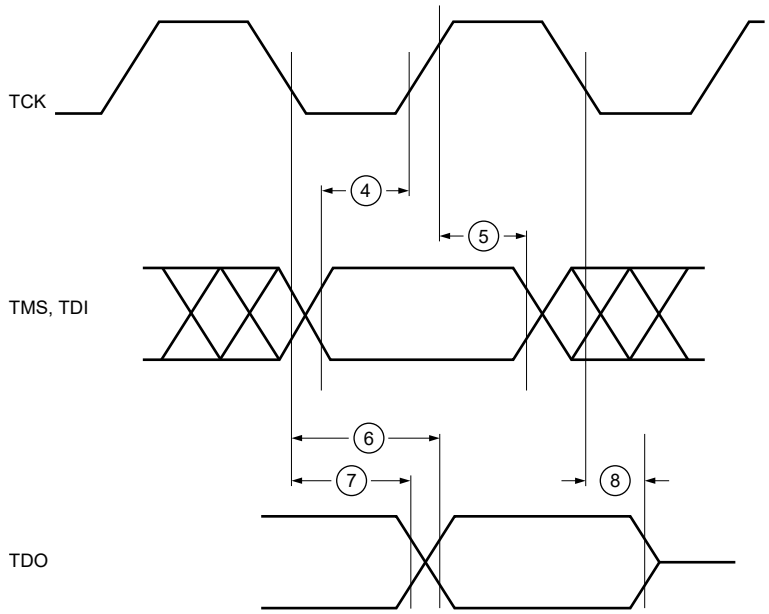

Figure 42. JTAG Test Access Port Timing

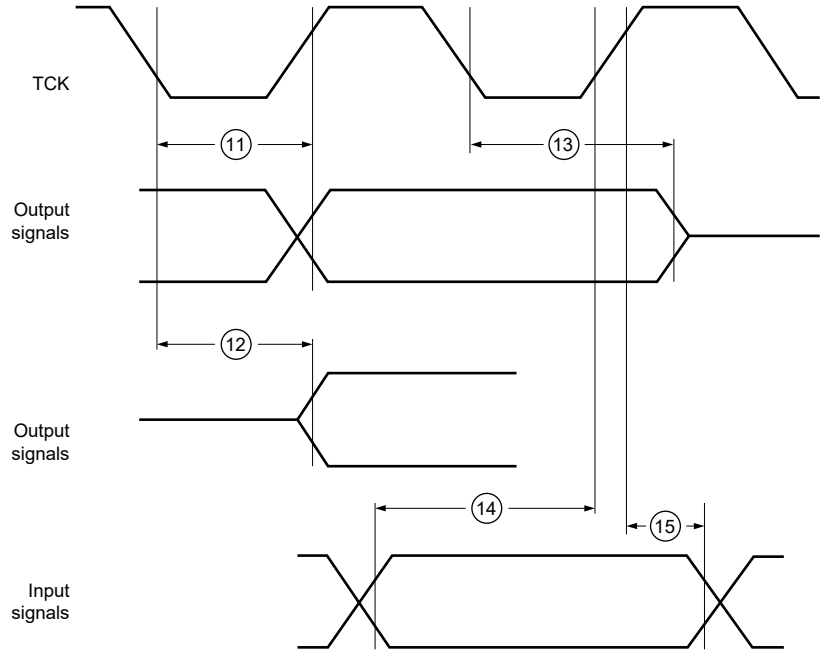

Figure 43. Boundary Scan Timing

17.3 SWD electrical specifications

The following table describes the SWD electrical characteristics. Measurements are with maximum output load of 30pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0.

Table 63. SWD electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S1	SWD_CLK frequency	—	—	33	MHz	—	S1
S2	SWD_CLK cycle period	1 / S1	—	—	ns	—	S2
S3	SWD_CLK pulse width	40	—	60	%	—	S3
S4	SWD_CLK rise and fall times	—	—	1	ns	—	S4
S9	SWD_DIO input data setup time to SWD_CLK rise	5	—	—	ns	—	S9
S10	SWD_DIO input data hold time after SWD_CLK rising edge	5	—	—	ns	—	S10

Table continues on the next page...

Table 63. SWD electrical specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S11	SWD_CLK high to SWD_DIO output data valid	—	—	22	ns	—	S11
S12	SWD_CLK high to SWD_DIO output data hi-Z	—	—	22	ns	—	S12
S13	SWD_CLK high to SWD_DIO output data invalid	0	—	—	ns	—	S13

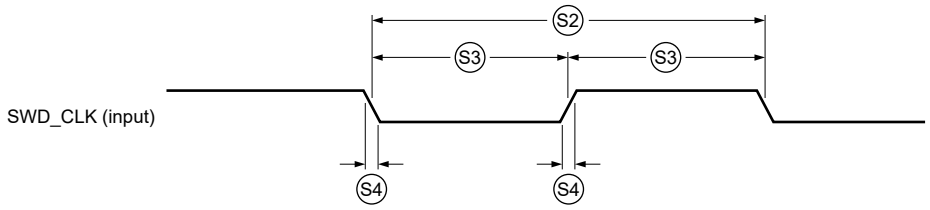

Figure 44. SWD Input Clock Timing

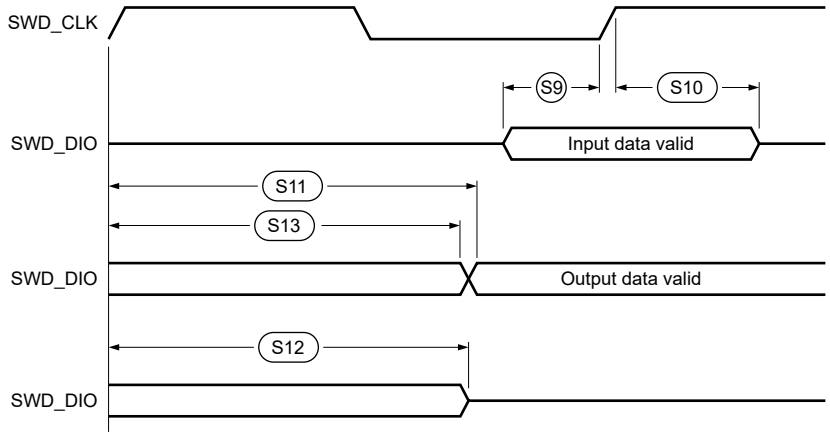

Figure 45. SWD Output Data Timing

18 Thermal Attributes

18.1 Description

The tables in the following sections describe the thermal characteristics of the device.

18.2 Thermal Characteristics

Thermal Design and Characteristics

- Junction temperature of the device does not solely depend on package thermal resistance but is also a function of chip power dissipation, PCB attributes, environmental conditions (ambient temperature & air flow) and cumulative effects of other heat generating ICs on the PCB.

- The appropriate thermal design must be carried out on package so that it can safely dissipate the necessary amount of power needed for it to function properly. This may involve adding a cooling solution on the package, creating thermal enhancements on the PCB and improving environmental conditions.
- The customer is encouraged to use the package model to perform design and risk assessment through simulations. Package models in FloTHERM or Icepak formats can be obtained under NDA from the sales team.

Thermal Ratings

- The table below is the S32K396 package thermal ratings for both MAPBGA and LQFP-EP package variants. These numbers are derived through simulations based on standardized tests as described in the footnotes.
- Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment :

Table 64. Thermal Characteristics

Rating	Board Type[1]	Symbol	Value by Package Type		Unit
			MAPBGA 289 I/O	LQFP-EP 176 I/O	
Junction to Ambient Thermal Resistances[2]	2s2p	$R_{\theta JA}$	22.5	19.4	°C/W
Junction-to-Top of Package Thermal Characterization Parameter [2]	2s2p	Y_{JT}	0.4	0.7	°C/W
Junction to Case Thermal Resistance (top)[3]	N/A	$R_{\theta JCtop}$	7.2	N/A	°C/W
Junction to Case Thermal Resistance (bottom)[4]	N/A	$R_{\theta JCbottom}$	N/A	1.8	°C/W

1. Thermal test board meets JEDEC specification for this package (JESD51-9 for MAPBGA and 51-7 for LQFP-EP). Test board has 7x7 via array under the package.
2. Determined in accordance with JEDEC JESD51-2A natural convection environment.
3. Junction-to-Case (top) thermal resistance determined using an isothermal cold plate. Case temperature refers to the MAPBGA's mold surface temperature.
4. Junction-to-Case (bottom) thermal resistance determined using an isothermal cold plate. Case temperature refers to the exposed pad surface temperature of LQFP-EP.

19 Dimensions

19.1 Obtaining package dimensions

Package dimensions are provided in the package drawings. To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

Package option	Document Number
176-pin LQFP-EP	98ASA01825D
289-ball MAPBGA	98ASA01216D

20 Revision history

The following table lists the changes in this document.

Rev 3, Mar 2024
• Updated the 6th character in Ordering Information • Updated the footnote attached to HVD_V15 symbol in Supply monitoring section • ADded L_SMPS and D_SMPS in V15 regulator (SMPS option) electrical specifications table • Updated Supply Currents section • Added ILKG_33_TWINANAMUX and ILKG_50_TWINANAMUX and removed ILKG_GPI, ILKG_50_I and ILKG_33_I from 3.3 V GPIO DC electrical specifications section and 5.0 V GPIO DC electrical specifications • Added footnotes to 3.3 V GPIO AC electrical specifications and 5.0 V GPIO AC electrical specifications table • Added Reference load diagram in 3.3 V GPIO AC electrical specifications section and 5.0 V GPIO AC electrical specifications section • ADded footnote that states "Value in the table represents .....external circuitry" to symbols of eTPU timing, eMIOS timing and LCU timing • Updated existing values and added parameters at 20 MHz frequency in Sigma Delta Analogto Digital Converter table • Updated CMRR value from 55 dB to 34 dB • Updated maximum frequency of FPLL_out and FPLL_vcoRange in PLL table • In LPSPI section — Updated the first point above table to "All timing is shown with respect to 50% VDD_HV_A/B thresholds" — Updated second point above table to "All measurements are with maximum output load of 30pF, input transition of 1 ns and pad configured DSE = 1, SRC = 0" — Updated min values of tLEAD/tLAG to ""tSPCK/2" for LPSPI Slave mode — For "tWPSCK", removed "high or low" from description — Removed Rise/Fall time output specs — Added footnotes "Output rise/fall time is determined by the output load and GPIO pad drive strength setting..." and "The input rise/fall time specification applies to both clock and data..." — Updated LPSPI Master Mode Timing (CPHA=0) and LPSPI Master Mode Timing (CPHA=1) figure • In LPSPI0 20 MHz and 15 MHz Combinations section, added note "LPSPI0 20 MHz and 15 MHz Combinations" • IN LPSPI Pad type table, removed PTF25 and updated PTA16 to PTA6 • Added note "QuadSPI cannot be used along with ENET in 176LQFP" in Ethernet MII (10/100 Mbps) section, Ethernet MII (200 Mbps) section and Ethernet RMII (10/100 Mbps) section • Added t2 and t3 in Microsecond channel • Updated 176 LQFP_EP package to "Yes" in Run Mode configuration • Updated ILKG_50_M0 LSL from -1614.4nA to -1615nA in 5.0 V GPIO DC Electrical specifications section • Updated the footnotes of LCU skew characteristics, eTPU skew charactteristics and eFlexPWM skew characteristics

Rev 2, Aug 2023
• Updated the title of datasheet to "S32K39 and S32K37 datasheet"

Table continues on the next page...

Rev 2, Aug 2023
• Updated the S32K38 part to S32K37 part all over the datasheet • Removed I3C feature all over the datasheet • Updated the S32K396 product series section • Updated mention of "GHzPWM configuration" to "eFlexPWM configuration" in Feature Comparison and Feature Summary • Added Clocks section in Feature Summary • Updated Feature Summary table • Updated "4x arm Cortex" to "3x arm Cortex" in both block diagrams and Feature Comparison section • Updated "arm" to "Arm" in both block diagrams • Updated 100 Mbps Ethernet to 10/100 Mbps Ethernet • Added Supported voltage supply use-cases, LPSPI Pad Type, and eMIOS • Added LCU skew characteristics, eTPU skew characteristics and eFlexPWM skew characteristics • Updated the maximum value of V15, description of V11 and added footnote ""Voltage at VDD_DCDC cannot be higher than VDD_HV_A" in Absolute maximum ratings to VDD_DCDC • In Voltage and current operating requirements — Added footnote to V15 as "Min and Max values are applicable only for non-SMPS mode where V15 is sourced externally". — Updated footnote from “VDDA_SWG must be shorted to VDD_HV_A at the PCB level” to “Must be shorted to VDD_HV_A at the PCB level” and add it to VDD_SDADC — Updated footnote from “SDADC can be only used when VDD_HV_A is 5V, otherwise SDADC cannot be used” to "SDADC is intended to be used only when VDD_HV_A is supplied with 5V. In case of VDD_HV_A is supplied with 3.3V it is recommended to disable SDADC in MC_ME module" and added to VREH_SDADC_xx — Added footnote "All the VREFH_xx except of VREFH_R2R must be shorted to single supply source at the PCB level, either isolated voltage reference or shorted to VDD_HV_A. Isolated VREFH_R2R is required to avoid SDADC performance degradation. If isolated supply cannot be used, then appropriate filtration is needed to isolate the VREFH_R2R noise." and attached to VREFH_R2R, VREFH_SDADC_xx and VREFH_SAR_xx. — Updated the footnote attached to VREFH specs to "VREFH should always be equal to or less than VDD_HV_A +0.1.." — Added IINJ_LVDS parameter specs with 100 µA as typical — Added footnote "Voltage at VDD_DCDC cannot be higher than VDD_HV_A" to VDD_DCDC • Added footnote to HVD_V15 in Supply Monitoring • In Recommended Decoupling Capacitors — Added "Only needed when internal SMPS is used to generate V15 and VDD_DCDC is supplied with isolated source from VDD_HV_A or VDD_HV_B" — Removed COUT_V15 parameter from Recommended Decoupling Capacitors and added in V15 regulator (SMPS option) electrical specifications as COUT_V15_SMPS — Added CBULK_SMPS with 22 µF as typical value

Table continues on the next page...

Rev 2, Aug 2023
— Updated the figures • Updated the title name of V15 regulator (SMPS option) electrical specifications and V11 regulator (NMOS ballast transistor control) electrical specifications • In V11 regulator (NMOS ballast transistor control) electrical specifications. split VTH_NMOS for 3.3 V supply and 5 Vsupply • Updated the typical value of V15 Output from 1.51 to 1.5 in V15 regulator (SMPS option) electrical specifications • Updated the description of V15 to "V15 Input" and typical value to 1.5 in V11 regulator (NMOS ballast transistor control) electrical specifications • Added V11 output with 1.14 typical value in V11 regulator (NMOS ballast transistor control) electrical specifications • In Supply currents section — Added column for VDD_HV_B in Example RUN mode configuration supply currents table — Removed Clock Option E column from Low speed RUN mode supply currents table — Removed "RUN mode supply currents (peripherals disabled)" table • Updated eFLEXPWM to 12 channels and eMIOS to 6 channels in RUN mode configuration options table in Operating mode • Updated GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V) and in GPIO DC electrical specifications, 5.0V (4.5V - 5.5V) • Updated 3.3V (2.97V - 3.63V) GPIO Output AC Specification and 5.0V (4.5V - 5.5V) GPIO Output AC Specification • Added eTPU timing diagram in eTPU timing • In LVDS 3.3V Transmitter Electrical Specifications and LVDS 5V Transmitter Electrical Specifications, updated the symbol of Deterministic Jitter from Eye_Jitter to Dj • In LVDS 5V Transmitter Electrical Specifications, updated min of Ipin_leakage to -5.6 and max to 5.6 and updated the unit of Dmax from MHz to Mbps • In SAR_ADC section, updated paragraph "All below specs are applicable...". and added footnote to TUE as "Spec valid if potential difference between VDD_HV_A.." and figure updated to show VDD_HV_A instead of VREF • In eFlexPWM, added "only for single instance" in Condition column of IVDD current consumption • Updated the values of Sigma Delta Analog to Digital Converter • In LPCMP section changed ACMP0 to LPCMP0 and updated the information after the table • In Sine wave generator, updated the footnotes and updated the minimum value of APP to 0.394 to be similar to minimum value of MINAPP • In Fast External Oscillator (FXOSC) — Updated IFOSXC, added EXTAL_SWING_PP, added CLKIN_VIL_EXTAL_BYPASS, CLKIN_VIH_EXTAL_BYPASS specifications and VSB specs and related footnote — Added two notes after the table • Updated section and table name from "Ethernet MII (100 Mbps)" to "Ethernet MII (10/100 Mbps)" and "Ethernet RMII" to "Ethernet RMII (10/100 Mbps)" • In Ethernet MII (10/100 Mbps)

Table continues on the next page...

Rev 2, Aug 2023
— Added 10/100 Mbps as Condition for RXCLK frequency, MII3, MII4 and TXCLK frequency — Updated the typical value of RXCLK frequency and TXCLK frequency to 2.5/25 — Added 10/100 Mbps as Condition for RMII input clock frequency • Updated SPIsection — Added "DRE=1 and SRE=0....timing" before table — Added Note "This modules corresponds with DSPI in RM" — Removed tA and tDIS and updated load capacitance from 25 pF to 30 pF • In Microsecond channel (MSC) — ADded footnote to MSC_GPIO stating "if MSC functionality is not used it can be used as SPI interface" — Added Note "This modules corresponds with DSPI in RM" — Added t1 with min as -1 and max as 1 ns — Updated the minimum values of tSCK (LVDS) to 25 and tSCK (GPIO) to 40 — Removed the parameter tCSC and tASC and added parameter tCSV and tCSH in — Updated the maximum value of tSCV to 26 ns(GPIO) and minimum value tSCH to -4 ns • Removed auto-learning mode from QuadSPI Octal 3.3V DDR 120MHz table • In PLL, updated the footnote to "For SSCG, jitter due to systematic modulation needs to be added as per applied modulation. Accumulated jitter specification is not valid with SSCG." • Added sentence before the table in PLL • Added accumulated and period jitter specifications in PLL table • In LFAST PLL table, updated the typical value of Rj to 50 ps. Updated the typical value of Dj to 80 ps and maximum value to 500 ps and added footnote "DJ max jitter includes influence of edge aligned IO activity" • Added "Data transitions measured....mid-supply" in QuadSPI Octal 3.3V DDR 120MHz and QuadSPI Octal 3.3V DDR 120MHz

Rev 1.1, Aug 2022
• In section "Voltage and current operating requirements", added "contact NXP sales representative for Hardware design guidelines document/package". • Updated section "Sigma Delta Analog to Digital Converter" to remove TBDs and other updates. • In section "SAR ADC", removed TBD from RS (max) specification.

Rev 1, Aug 2022
• Updated data sheet classification to "Advance Information". • Updated sections S32K396 product series, feature comparison and feature summary. • In section "Absolute maximum ratings":

Table continues on the next page...

Rev 1, Aug 2022
— Updated V15 description as "Voltage sensing input". — Added voltage range for VDD_LVDS. • In section "Voltage and current operating requirements": — Added a note as "DSPI/MSC interface is supported only at VDD_HV_A = 5V." — Updated V15 description as "Voltage sensing input". — Added footnote to VDDA_SWG as "VDDA_SWG must be shorted to VDD_HV_A at the PCB level." — Added voltage range for VDD_LVDS and footnote "Ensure that VDD_HV_A ramps before VDD_LVD.". — Added VDD_SDADC supply. — ADC reference voltage symbol and description updated. — Removed 3.3 V from SD ADC reference voltage typical, updated minimum and added a footnote as "VREFH_SDADC_xx must be shorted to single supply source...". — Added R2R high/low voltage reference specifications. • Deleted LVD_V15 from "Supply monitoring"" • In section "Recommended Decoupling Capacitors": — Updated description of CDEC and a related footnote updated to mention 10nF instead of 1 nF Optionally, 10 nF capacitors can be added...". — Decoupling capacitors pinout diagrams updated. • In section "SMPS regulator electrical specifications": — Added "External schottky diode average forward current". — Added 2V as "External P-channel MOSFET threshold voltage". • In section "NMOS Ballast Transistor Control Specification" added CNMOS (NMOS gate stability capacitor) • Updated IDD tables in "Supply currents". • In section "Operating mode" changed I3C to I2C. • Added section "Cyclic wake-up current" • In section "GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)" deleted ILKG_33_S_PTE13. • In section "GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)" deleted ILKG_50_S_PTE13. • In section "LVDS 3.3V Receiver Electrical Specifications", added sentence "These specifications are related to LVDS pads dedicated to Zipwire." • Added "LCU"and "eTPU timing". • Changed "AE Nano Edge" to eFlexPWM. • In section "SAR SDC" — CP2 (all/standard channels) updated from 4.18 to 5 pF. — CP2 (precision channels) updated from 1.42 to 2.2 pF. — In footnote attached to TUE updated to mention 12-bit level resolution for both precision and standard channels. • In section "FXOSC" removed crystal recommendations and updated a paragraph as "To ensure stable oscillations, FXOSC...".

Table continues on the next page...

Rev 1, Aug 2022
• In section "LPSPI", updated part of sentence as "All measurements are with maximum output load of 30 pF...." and updated tV for Slave_10Mbps from 36 to 41 ns. • In section "MDIO timing specifications" updated MDC3 from 25 to 28 ns. • In section "I3C Push-Pull Timing Parameters for SDR Mode" added tDVO specs and updated tSU_PP from 3 to 5 ns. • Added sections "SPI" and "Microsecond channel (MSC)". • In section "QuadSPI Octal 3.3V DDR 120MHz": — Updated part of sentence as "QuadSPI trace length should be less than or equal to 2 inches.". — Updated tOD_DATA, tOD_CS, IH_DQS and deleted tDVW. • In section "QuadSPI Quad 3.3V SDR 120MHz": — Updated part of sentence as "QuadSPI trace length should be less than or equal to 2 inches.". — deleted specs related to internal loopback, updated tIS and tDVW • Added QuadSPI configurations.

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Date of release: 03/2024
Document identifier: S32K396