X-S32K148EVBQ144/Q176

CUSTOMER EVB

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Revisions

Rev	Description	Designer	Date	Approved
X4	Schematic	J.Sanchez		TBD
A	Prototype			
AX1	First Release			

CAUTION:

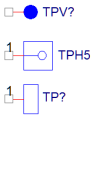
This schematic is provided for reference purposes only. As such, NXP does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the NXP S32K family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

3 Different test points used in design:

TPVx - Through Hole Pad small

TPHx - Through Hile Pad Large (for standard 0.1" header). Also used on IO Matrix (IOMx)

TPX - Surface Mount Wire Loop



Notes:

- All components and board processes are to be ROHS compliant
- All connectors and headers are denoted Jx/Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2.
  2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

User notes are given throughtout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS

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Designer: Jesus Sanchez	Drawing Title: X-S32K148EVB-Q176		
Drawn by: Jesus Sanchez	Page Title: TITLE		
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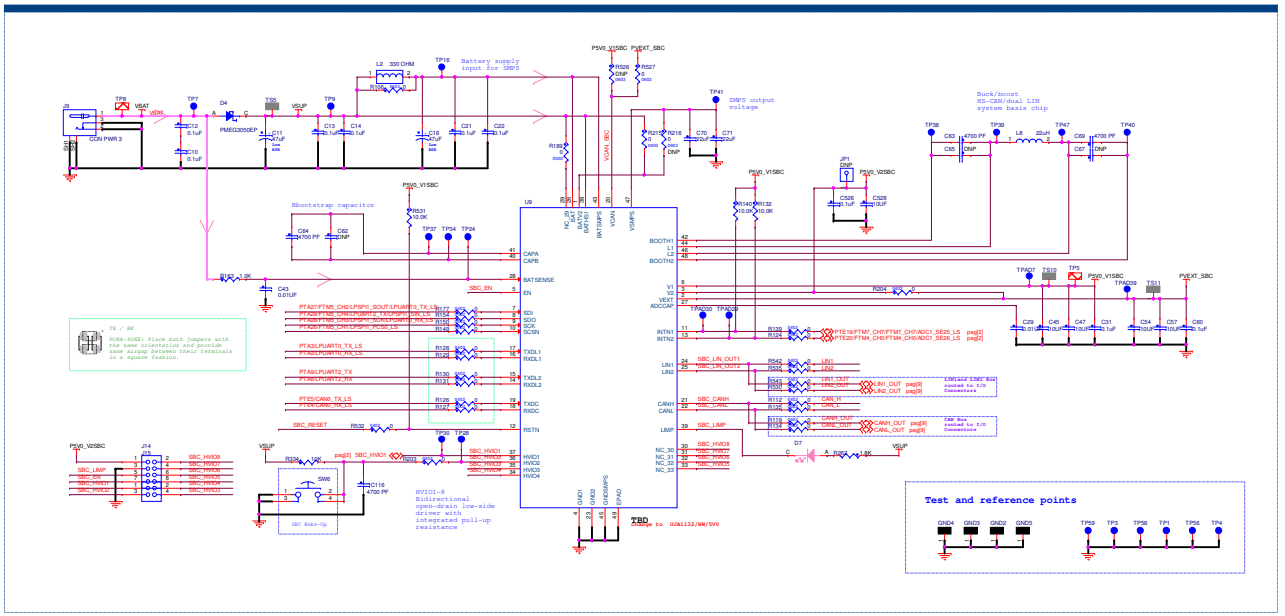

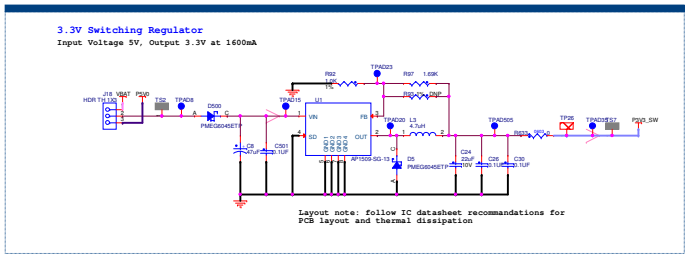

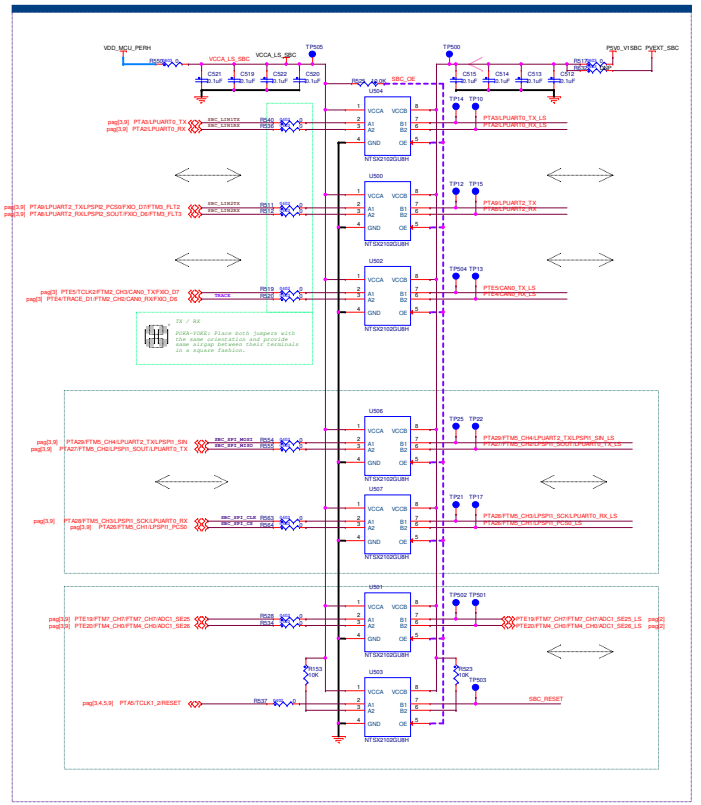

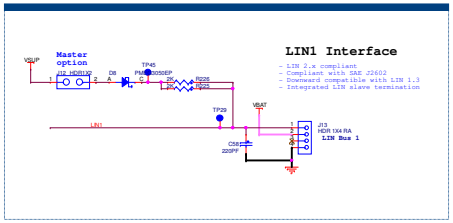

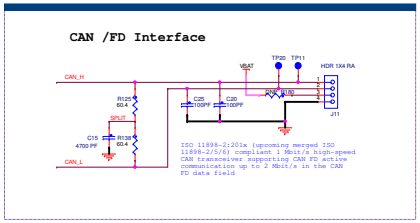

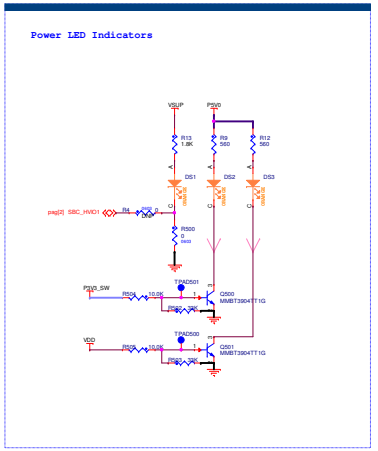

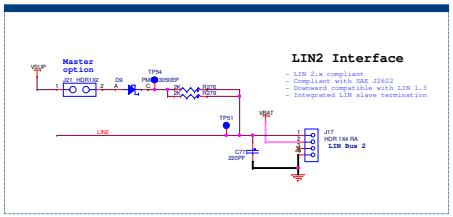

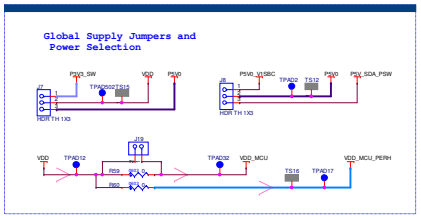

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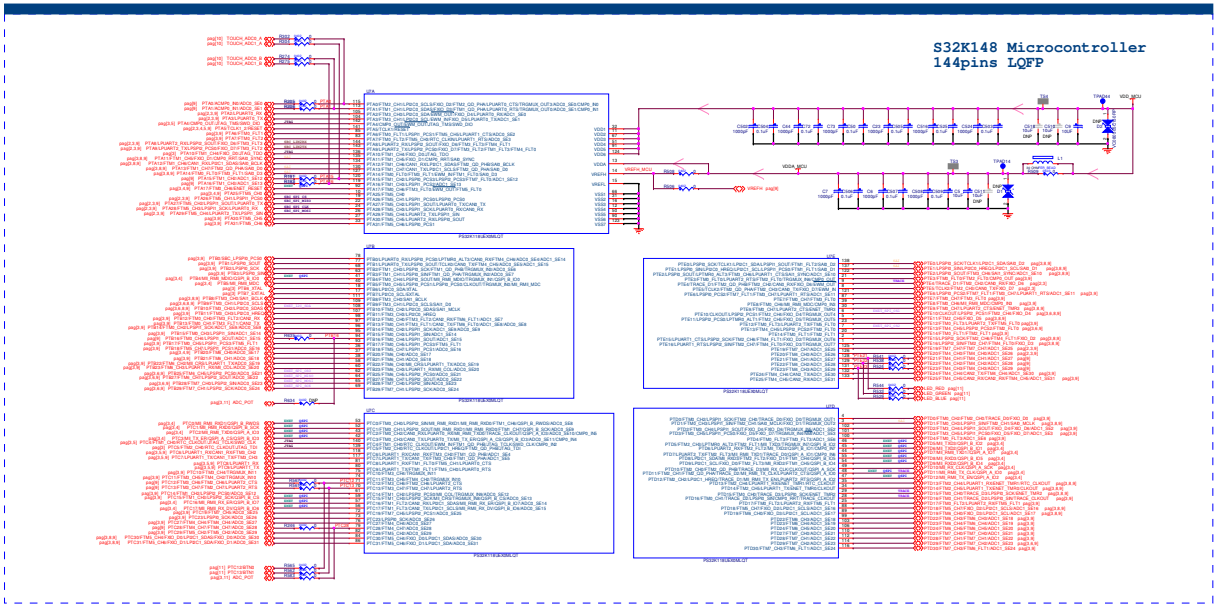

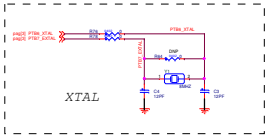

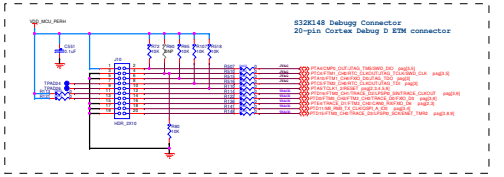

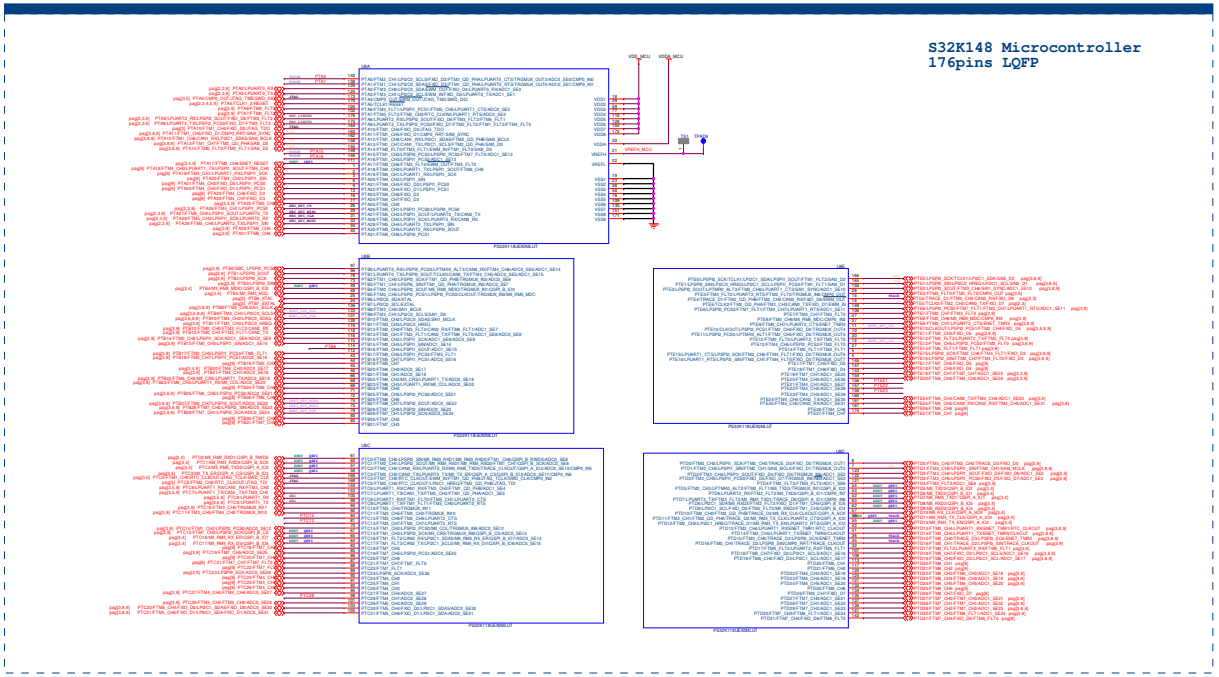

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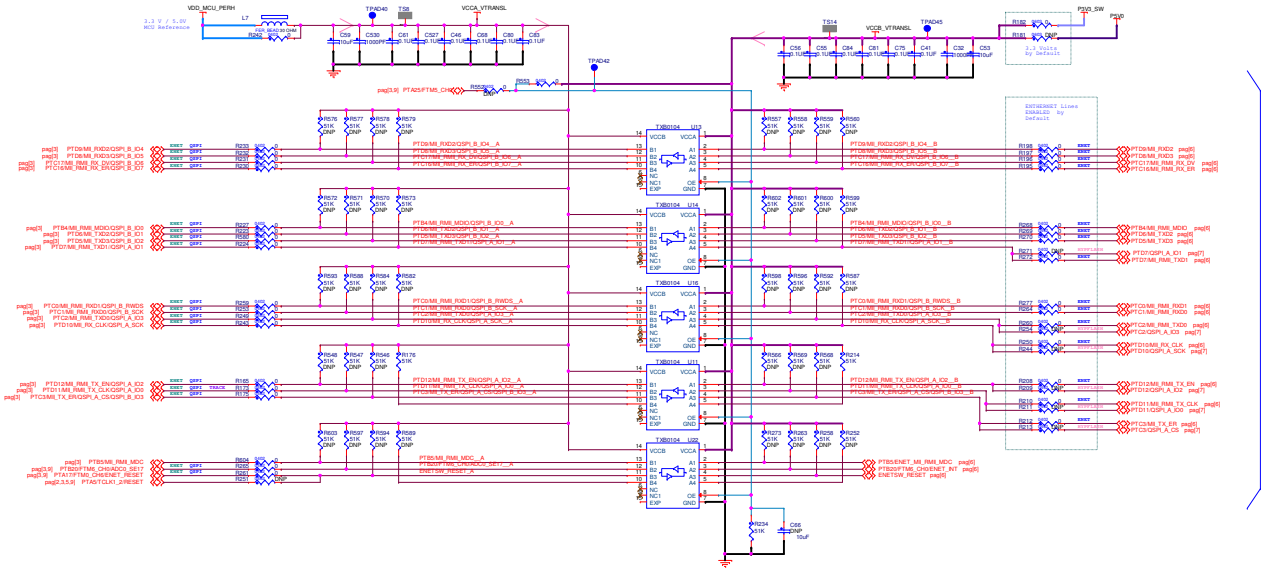
S32K148
MCU SIGNALS



HyperFLASH &
Ethernet Connector

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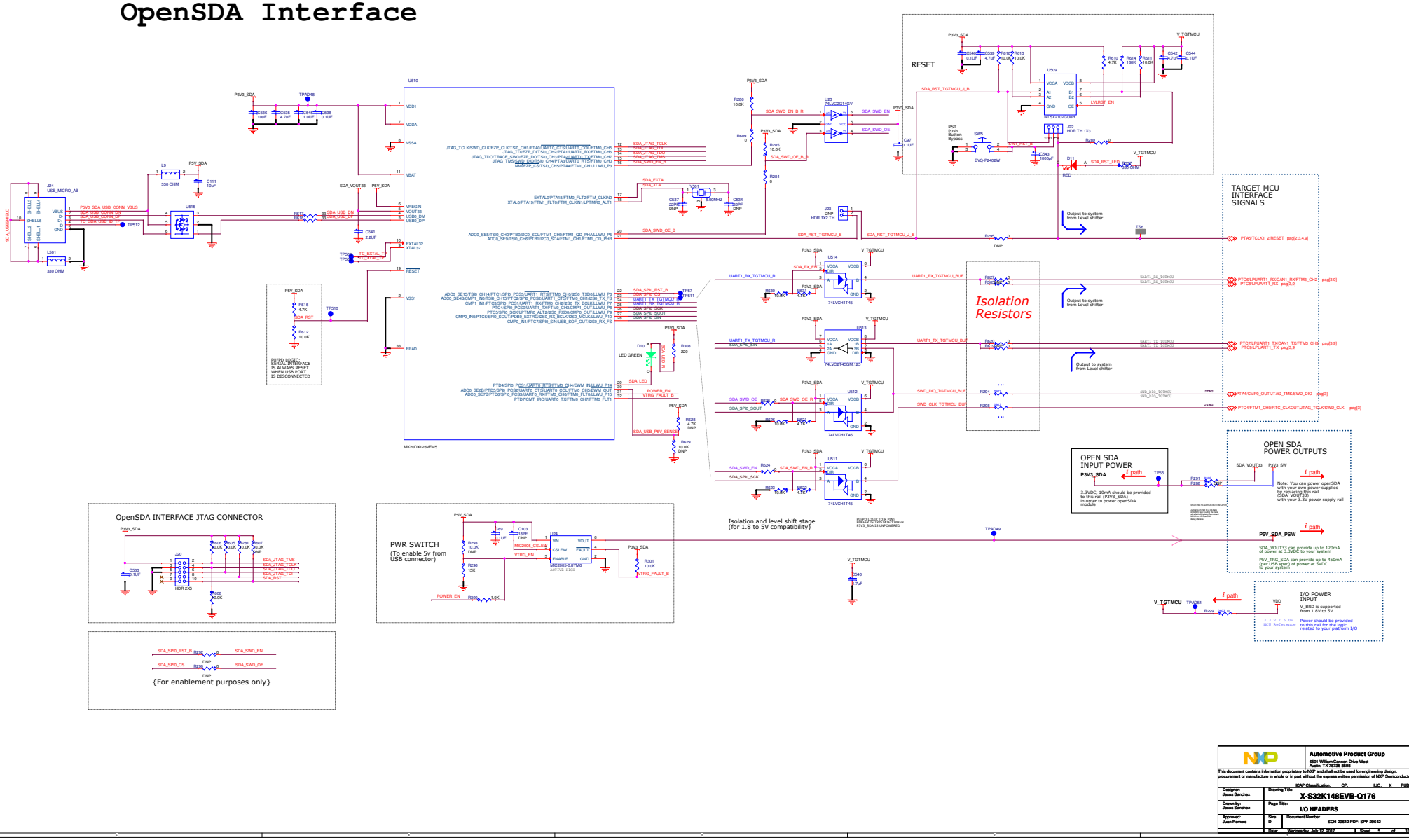
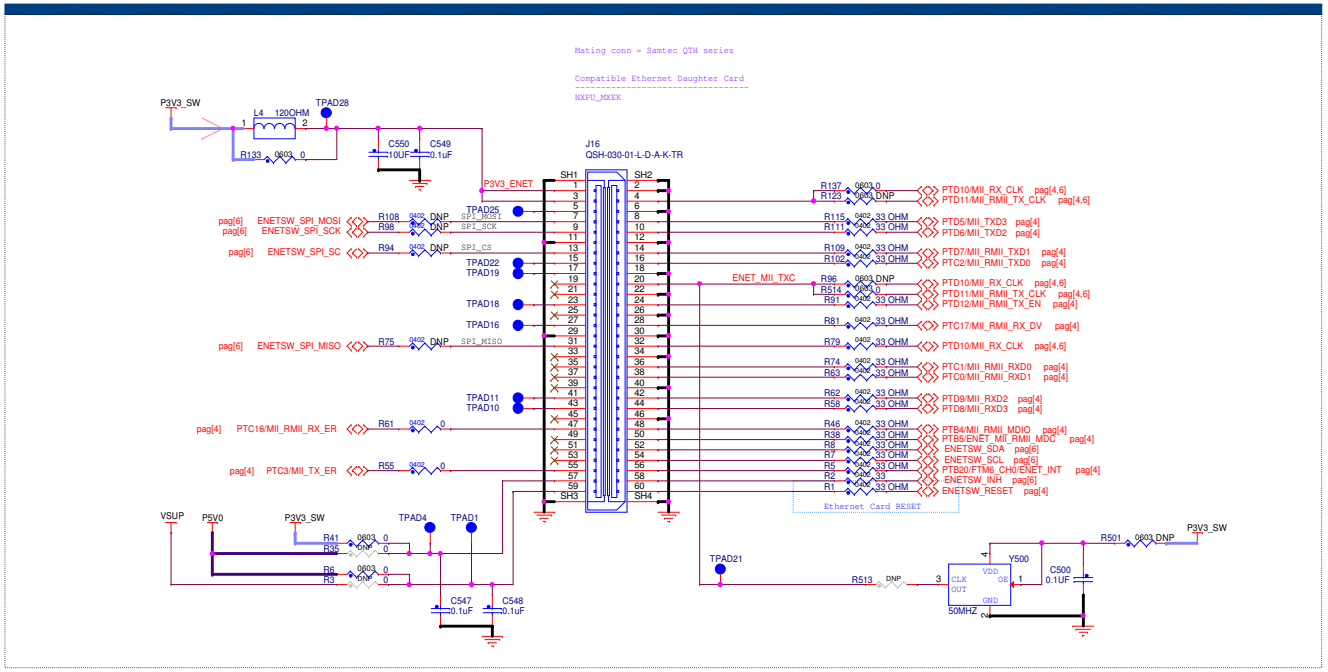
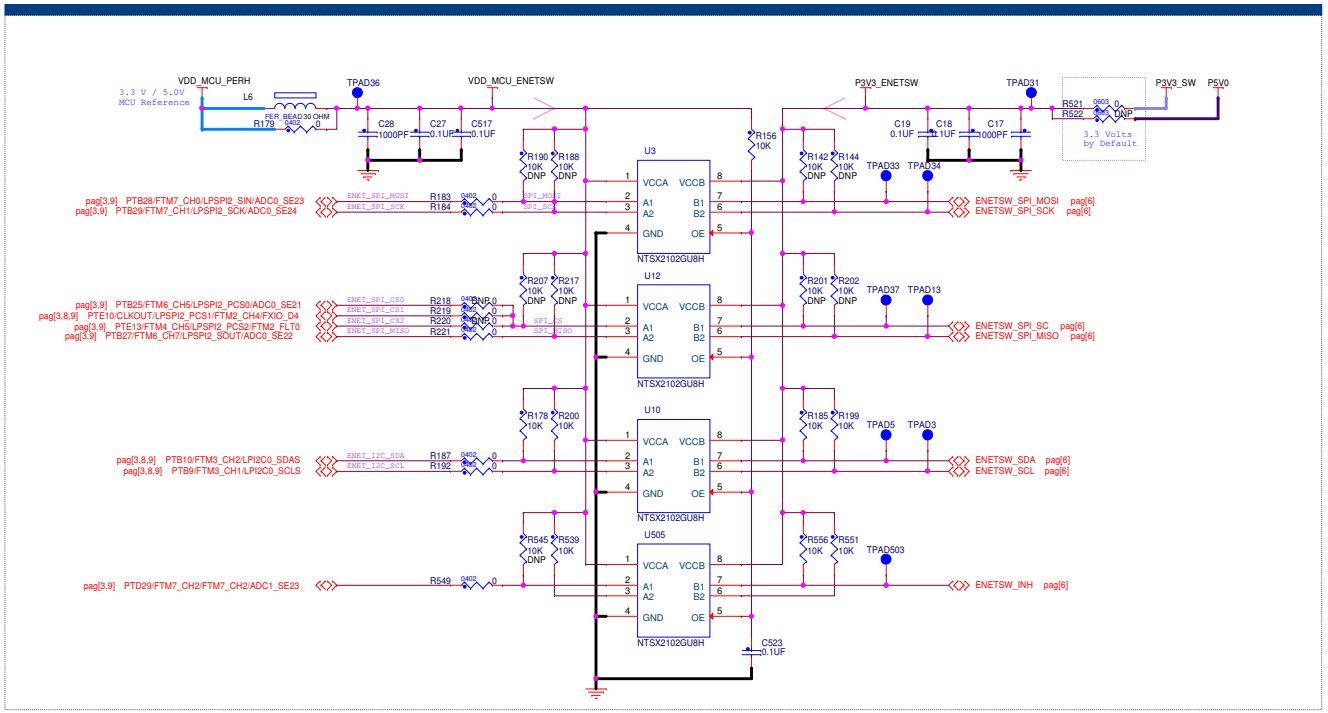
OpenSDA Interface







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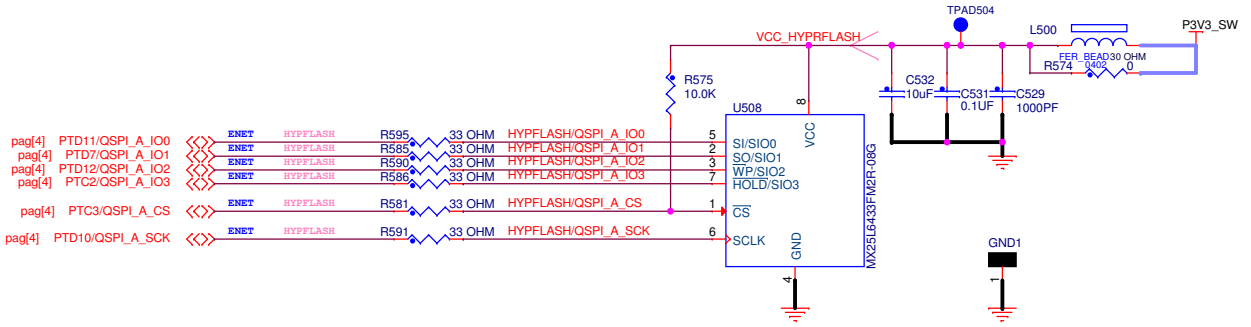
CMOS FLASH Memory 64M-BIT



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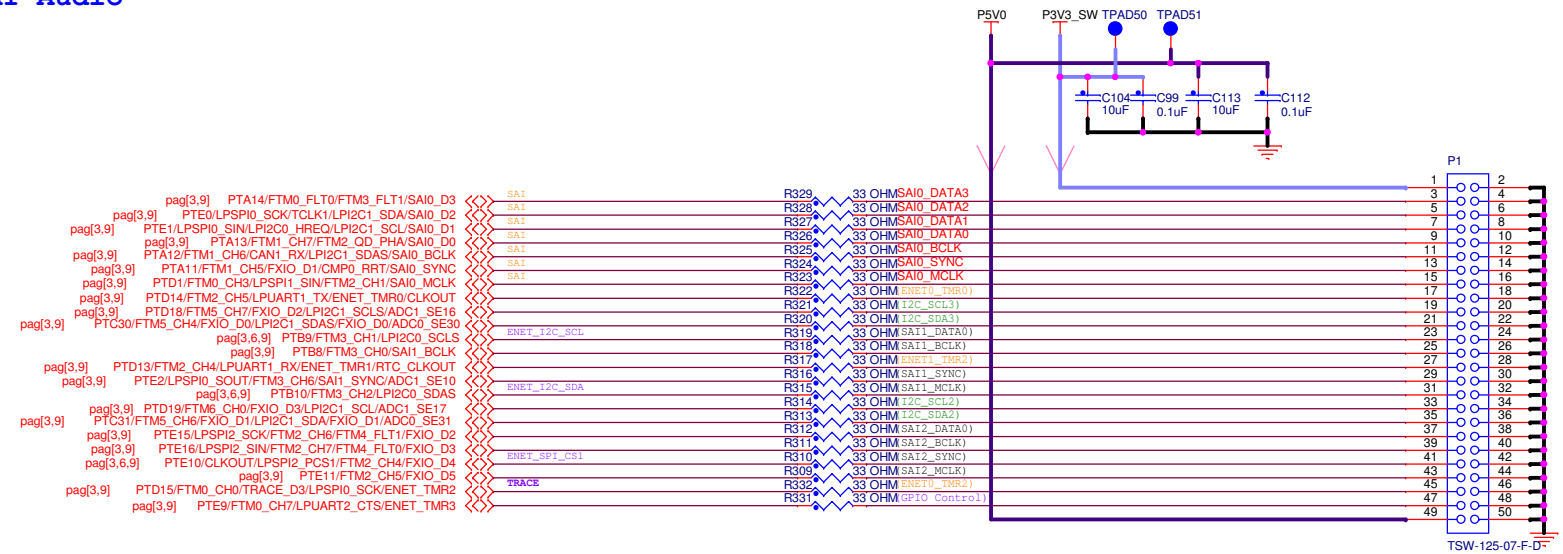
SAI Audio



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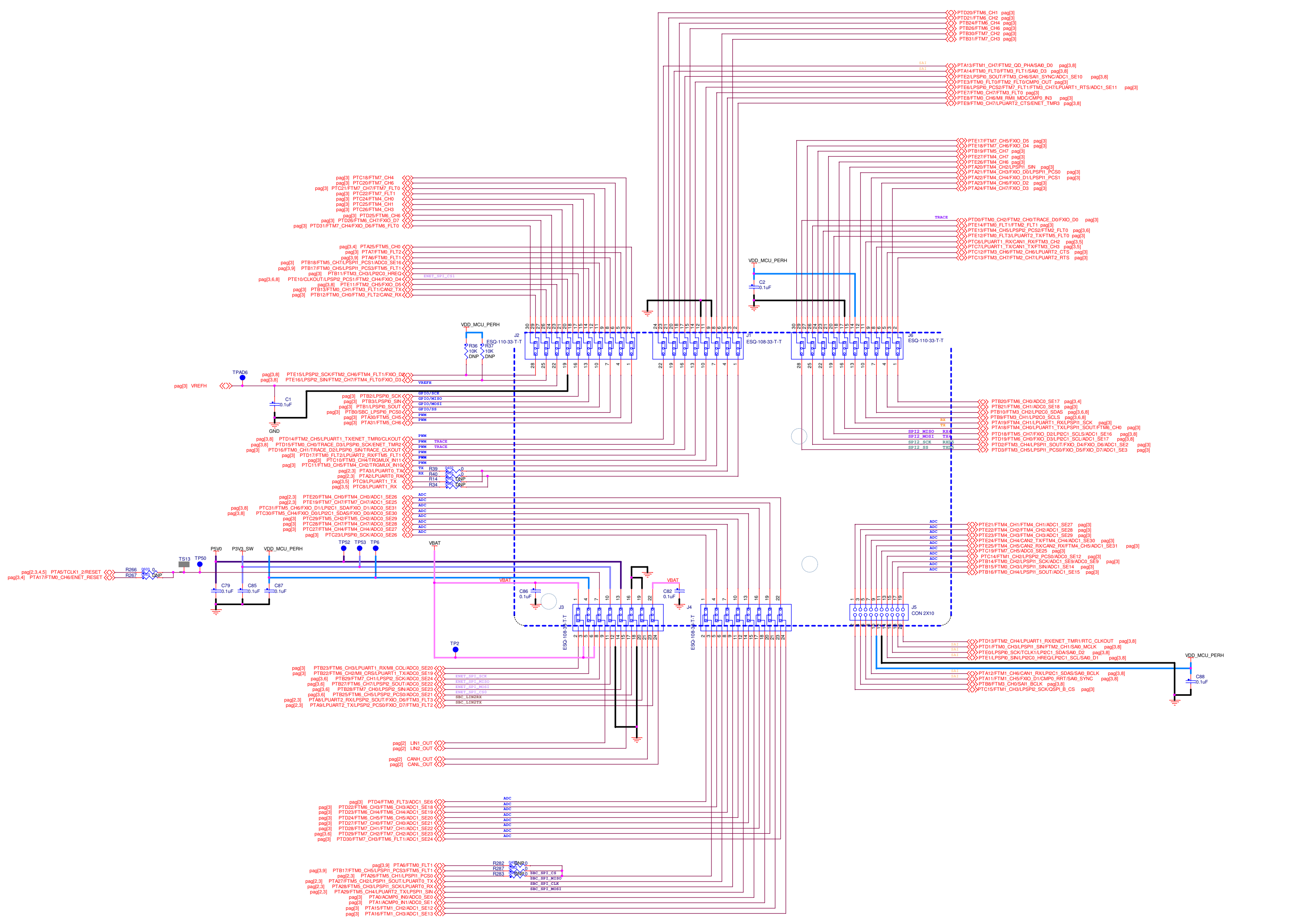

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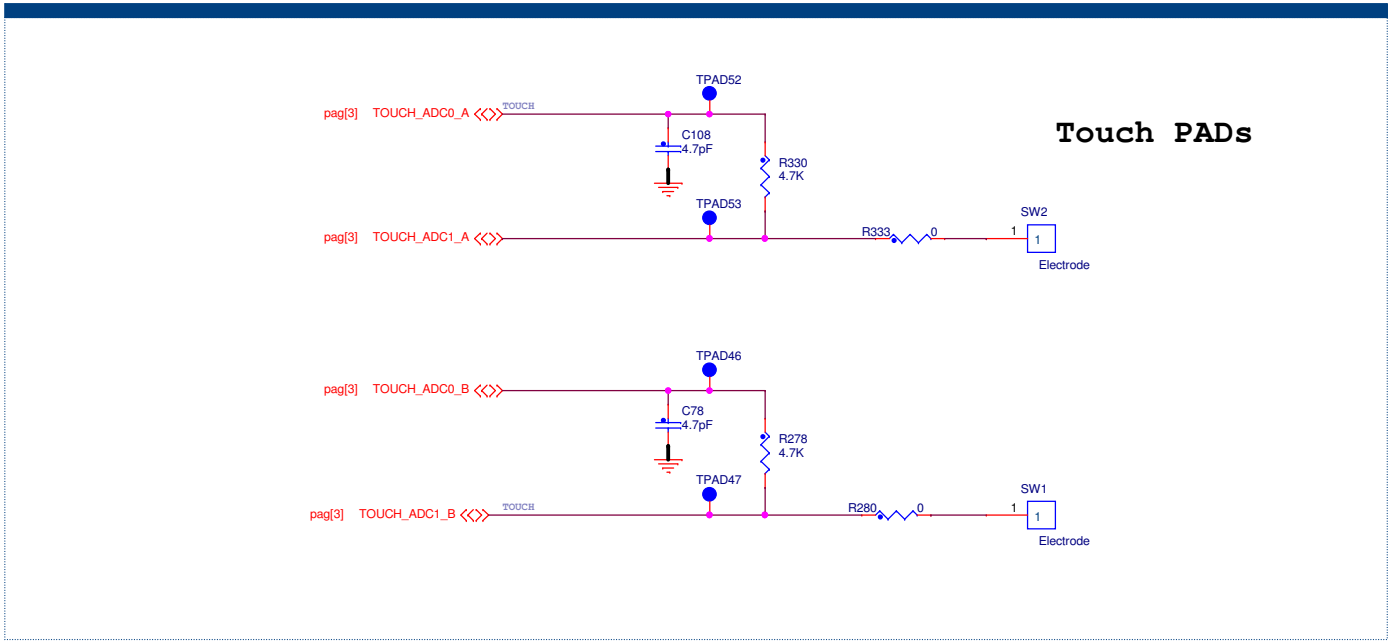

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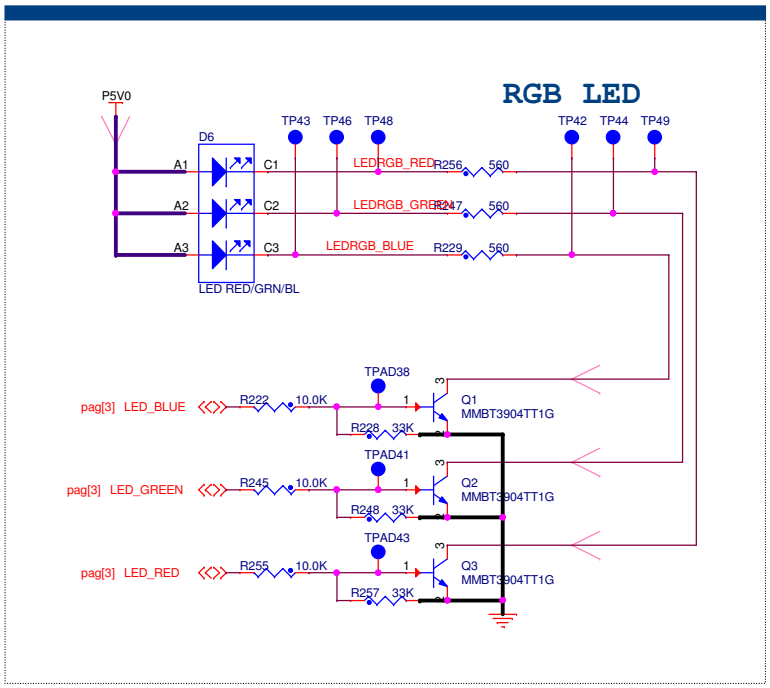

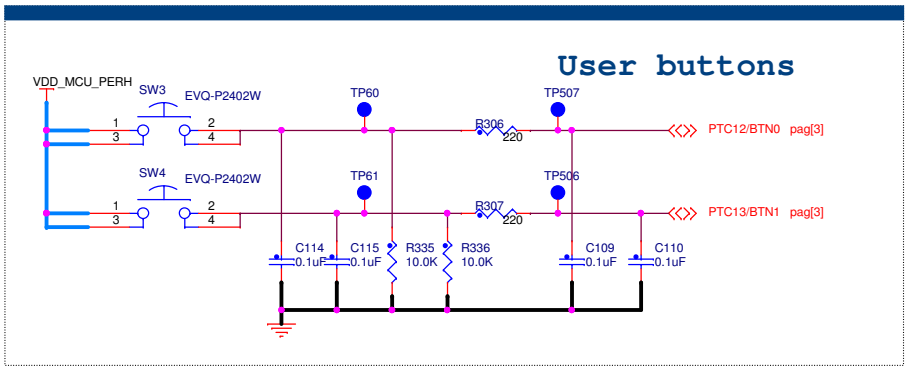

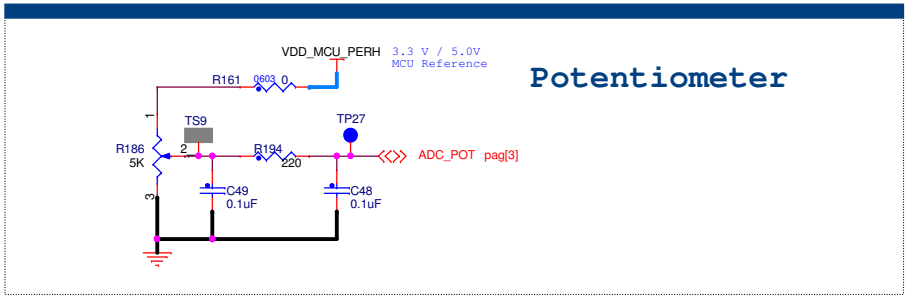

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